F81962/F81964/F81966/F81967

eSPI/LPC 2/4/6 UARTs Super I/O with 128 Bytes FIFO & Power Saving Functions

Release Date: Feb, 2018
Version: 0.18P

F81962/F81964/F81966 /F81967 Datasheet Revision History

Version	Date	Revision History
0.10P	Sep, 2015	Preliminary Version
0.11P	Dec, 2015	• Made Clarification and Modification • Update Function Description • Update Registers
0.12P	Sep, 2016	• Made Clarification and Modification • Add New Item F81967
0.13P	Nov, 2016	• Update Application Circuit
0.14P	Mar, 2017	• Made Clarification and Modification • Add new registers setting in section 5.1.11 and 5.8.27 • Add eSPI interface
0.15P	May, 2017	• Made Clarification and Modification • Add More Description of CLKIN • Update Application circuit
0.16P	July, 2017	• Made Clarification and Modification • Update WDT function update • Update Application circuit
0.17P	Aug, 2017	• Made Clarification and Modification • Update WDT function update • CLKIN program diagram update
0.18P	Feb, 2018	• Update Application Circuit for eSPI • Made Clarification and Modification

Table of Contents

1 General Description

The F81962/F81964/F81966/F81967 is the featured IO chip for Industrial PC system. Equipped with one IEEE 1284 parallel port, 6 UART ports with Multi drop function (9-bit protocol), SIR, 80 port, master SPI, ACPI management function. Each UART provides 16/32/64/128 bytes FIFO. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems. The F81962/F81964/F81966/F81967 supports the enhanced parallel port (EPP) and the extended capabilities port (ECP). The F81962/F81964/F81966/F81967 supports keyboard and mouse interface which is 8042-based keyboard controller. The F81962/F81964/F81966/F81967 integrated with hardware monitor, 7 sets of voltage sensor, 3 sets of creative auto-controlling smart fans and 2 temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external transistors 2N3906 and one local temperature.

The F81962/F81964/F81966/F81967 provides flexible features for multi-directional application. For instance, supports 80 GPIO pins, IRQ sharing function designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature. Others, the F81962/F81964/F81966/F81967 supports newest Intel PECI 3.0 interfaces for new generational CPU temperature usage, INTEL IBX PEAK, I2C and AMD TSI for temperature reading.

In order to save the current consumption when the system is in the soft off state which is so called power saving function. The power saving function supports the system boot-on not only by pressing the power button but also by the wake-up events via GPIO0x, GPIO1x, RI1#, and RI2#. When the system enters the S3/S4/S5 state, F81962/F81964/F81966/F81967 can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be emulated to G3-like state when the system enters S3/S4/S5 states. At the G3-like state, the F81962/F81964/F81966/F81967 consumes 5VSB power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfill a low power consumption system which supports a wake up function.

The F81962/964/966/967 are also suited for Skylake eSPI interface. The F81962/964/966/967 have eSPI and LPC interfaces where the interface would be detected automatically. Those interfaces could be workable with 1.8V or 3.3V. Also support master LPC interface (F81967 only) for Fintek LPC SIOs' usage.

These features as above description will help you more and improve the product value. The F81962/F81964/F81966/F81967 is in the package of 128-LQFP. (14mm*14mm)

2 Feature List

General Functions

- Comply With LPC 1.1 & eSPI 0.75 Interfaces
- Support Master LPC Interface (only for F81967) For Fintek SIOs' Usage Which Could Be Selected From UART 6 Or LPT Port where default is output from printer's data bus.
- Support ACPI
- Support WDT Reset Function
- Support WDT wake up while ERP function is enabled
- Provide 4 sets of GPIO (GPIO0x/1x/5x/8x) SMI event via PME# or SIRQ
- Provide different SIRQ channels for GPIO0x/1x/5x/8x
- Provide one KBC
- Provide Parallel Port (LPT) Which Could Be Divided Into Data And Signal Port Via Registers
- Support 80 Ports Which Could Be Selected From UART 6 Or LPT where default is output from printer's data bus.
- Support Master SPI Function Which Could Be Selected From UART 6 Or LPT where default is output from printer's data bus.
- Provide 6 fully functional UART and 1 SIR
  - Programmable 16/32/64/128 bytes FIFO
  - Multi drop function
  - Support IRQ Sharing
  - Provide auto flow control
- H/W monitor functions
  - Support OVP & UVP for 3VCC and VIN2&3
  - Support smart fan FQST for FAN 1
  - Support PECI 3.1
  - Support IBX PCH temperature reading via I2C
  - Support AMD TSI, MXM via I2C pins.
- 80 GPIO Pins for flexible application
- Support I2C Function Via Pin 55, 62, 68, 71 (SDA) & Pin 54, 61, 67, 76 (SCL)
- Provide Power Saving Function (Comply ERP lot 6.0)
- Support Intel Deep Sleep Well (DSW) Timing Sequence
- Provide wake-up events via power button, GPIO0x, GPIO1x, RI1#, and RI2#
- Provide ATX emulates AT function
- 24 /48 Mhz (Default) Clock Input, Others Clock Input Could Be Programmable Via Register
- Support Auto Re-Generates PWSOUT# Signal Only At Always On Or AT Mode
- Packaged in 128-LQFP

Bus Interface

- Comply With Intel's Slave LPC Interface Specification Revision 1.1
- Comply With Intel's Slave eSPI 1.0 Specification

Intel Platform

- Support Skylake eSPI/LPC Interface
- Support Intel® Deep Sleep Well (DSW)
- LRESET#/SIRQ Support Low Voltage Level for 1.8V

Hardware Monitor Management

- Monitoring hardware monitor functions under S3 could be disabled.
- Digital Thermal Interfaces
  - Intel® PECI 3.1 for Intel CPU thermal monitoring
    - ❑ 4 selectable PECI address 30h~33h
    - ❑ CPU address auto detect mode
  - Intel Ibex thermal monitoring
  - SB-TSI for AMD® CPU and MXM thermal monitoring
  - T1 and T2 beta compensation
- Analog Thermal Interface
  - 2 x Thermistor or Thermal Diode (BJT) connected to device ADC inputs
  - Support Dual Current Type (±3℃) thermal inputs
  - 1 x Local Temperature source

Temperature sensor can setting OVT limit and high limit

- Generates OVT#, PME#, BEEP or shutdown via hardware signals output on critical temperature events
  - OVT
    - ❑ Temperature over limit support max three source
    - ❑ Even output support level mode and pulse mode
    - ❑ Event output can indicate by 1Hz LED or 400/800Hz BEEP
  - ALERT
    - ❑ Even output support level mode and pulse mode
    - ❑ Event output can indicate by 1Hz LED or 400/800Hz BEEP
  - BEEP
    - ❑ Event output source support OVT or ALERT
- Fan Control and Monitor
  - 3 Auto PWM or DAC fan controls
  - 3 Fan speed monitoring inputs
  - Fan control support Stage Auto Mode (4-Limit and 5-Stage)/Linear Auto Mode/Manual Mode
  - Programmable hysteresis and setting points for all monitored items
  - Provide FAN real time status
  - Temperature over high limit FAN can force full speed
  - Programmable PWM mode up to 300 kinds of frequencies (15Hz~23.5KHz)
- 8 voltage monitoring and indication (VIN1, VIN2, VIN3, VIN4, 3VCC, 5VSB, 3VSB, VBAT)
  - Monitoring VBAT voltage could be disabled via the register.
  - Voltage-Protect Status
    - ❑ Over Voltage Protect (OVP) Limit: 3VCC, VIN1, VIN2, VIN3
    - ❑ Under Voltage Protect (UVP) Limit: 3VCC, VIN2, VIN3
  - Shut down when OVP/UVP occurred
    - ❑ 3VCC, VIN2 and VIN3
- Case intrusion detection (COPEN#)
  - Even output via Beep and PME at the same time

Power Management

- Comply with ERP Lot 6.0
- Support ACPI
- Support Intel Deep Sleep Well (DSW) state control
- Support G3 like state control
- Built in Two Control Pins with VSB Power Sources Control
- System Wake-Up Control
  - Optional routing of events to generate PME on detection of:
    - ❑ Keyboard key strokes
    - ❑ Mouse movement and/or button left click
    - ❑ Ring Indication RI1# and RI2# on the serial ports
- Provide ATX Emulates AT Function
- Support Auto Re-Generates PWSOUT# Signal Only At Always On Or AT Mode Which Would Be Auto Regenerated After 800ms Until S3# De-Asserted.

Glue Functions

- **LED status indication**
  - Programmable blinking at S0, S3, Deep S3, S5 state
  - Use Along With UART1~6
    - ❑ TX LED 1/2/3/4/5/6: Output Via DTR1/2/3/4/5/6#
    - ❑ RX LED1/2/3/4/5/6: Output Via DSR1/2/3/4/5/6#

- **Watch Dog Timer**
  - Time resolution minute/second
    - ❑ Maximum 256 minutes or 256 seconds
  - Time Out Signal Can Output Via WDTRST#, PWROK, PME#

Legacy Modules

- **UART**
  - F81962: 2High-Speed 16C550/16C650/16C750/16C850/16C950 Compatible UARTs
  - F81964: 4 High-Speed 16C550/16C650/16C750/16C850/16C950 Compatible UARTs
  - F81966/F81967: 6 High-Speed 16C550/16C650/16C750/16C850/16C950 Compatible UARTs

Programmable 16/32/64/128-Byte Send/Receive FIFO Depth
Support RS232, RS422 and RS485
RS485 Mode
- ❑ Auto Flow Control

RS232 Mode
- ❑ Hardware Auto Flow Control With via DTR# or RTS#

Baud Rate
- ❑ Baud Rate Supports 115.2 Kbps, Up To 1.5 Mbps
- ❑ Programmable Baud Rate

Support IRQ 3,4,5,6,7,8,9,10,11 Sharing
Provide Multi Drop (9-Bits) Function For Gaming Machine
Support Ring-In Wake Up Via RI1# And RI2#

- **Infrared**
  Support IrDA 1.0 SIR protocol (Multi with Com 6)
  Maximum baud rate up to 115.2K bps

- **Parallel Port(LPT)**
  One PS/2 compatible bi-directional parallel port
  Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284
  Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284
  Enhanced printer port back-drive current protection

- **80-Port Interface**
  Monitor 0x80 Port And Output The Value Via Signals Defined For 7-Segment Display.
  High Nibble And Low Nibble Are Outputted Interleaved At 1KHz Frequency.
  80-Port Is Programmable Via UART 6 Or LPT
  Temperature Data Could Be Output Via 80 Port
  Enable Via Power On Strapping Pin Or Register.

- **Master SPI Interface**
  Support 8 Clock & 8 Bit Data.
  CS# Could Be Kept Low Or Return To High Stage.
  Programmable Via UART 6 Or LPT where default is output from printer's data bus.

- **PS/2 Keyboard and Mouse Controller (KBC)**
  Support Keyboard/Mouse wakeup and swap function
  Compatibility with the 8042
  Hardware Gate A20 and Hardware Keyboard Reset

- **General-Purpose Input/ Output**
  80 GPIO pins, all GPIOs individually configured as input or output
  GPIO0x and GPIO1x support interrupt status (wake up)
  GPIO0x, GPIO1x, GPIO5x and GPIO8x support different SIRQ channels
  GPIO1x Supports 8 Functions: GPIO (default), PME#, CLKOUT, BEEP, LED_VCC, LED_VSB, WDTRST#, ALERT#
  CLKOUT = 48MHz / (CLKOUT_PRE_DIV * 2), where CLKOUT would be 48/24/12/8MHz → Index 2Bh (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 1), bit 5-4

Clocking, Supply and Package Information

- Clocks
  CLKIN supports 24 /48 MHz (default) clock input, others clock could be programmable internally via register.
- Power Supply
  1.8V VCC For ESPI Bus Operation
  1.8V/3.3V VCC For LPC Bus Operation
  5VSB, 3VCC, 3VSB, VBAT
- Package
  128-PIN LQFP (14mm*14mm) Green Package
  Operation Temperatures Range -40°C ~ 85°C

Patented TW207103 TW207104 TW220442 US6788131 B1 TWI235231 TW237183 TWI263778

3 Pin Configuration and Description

3.1 Pin Configuration

Figure1. F81967 pin configuration (14mm*14mm)

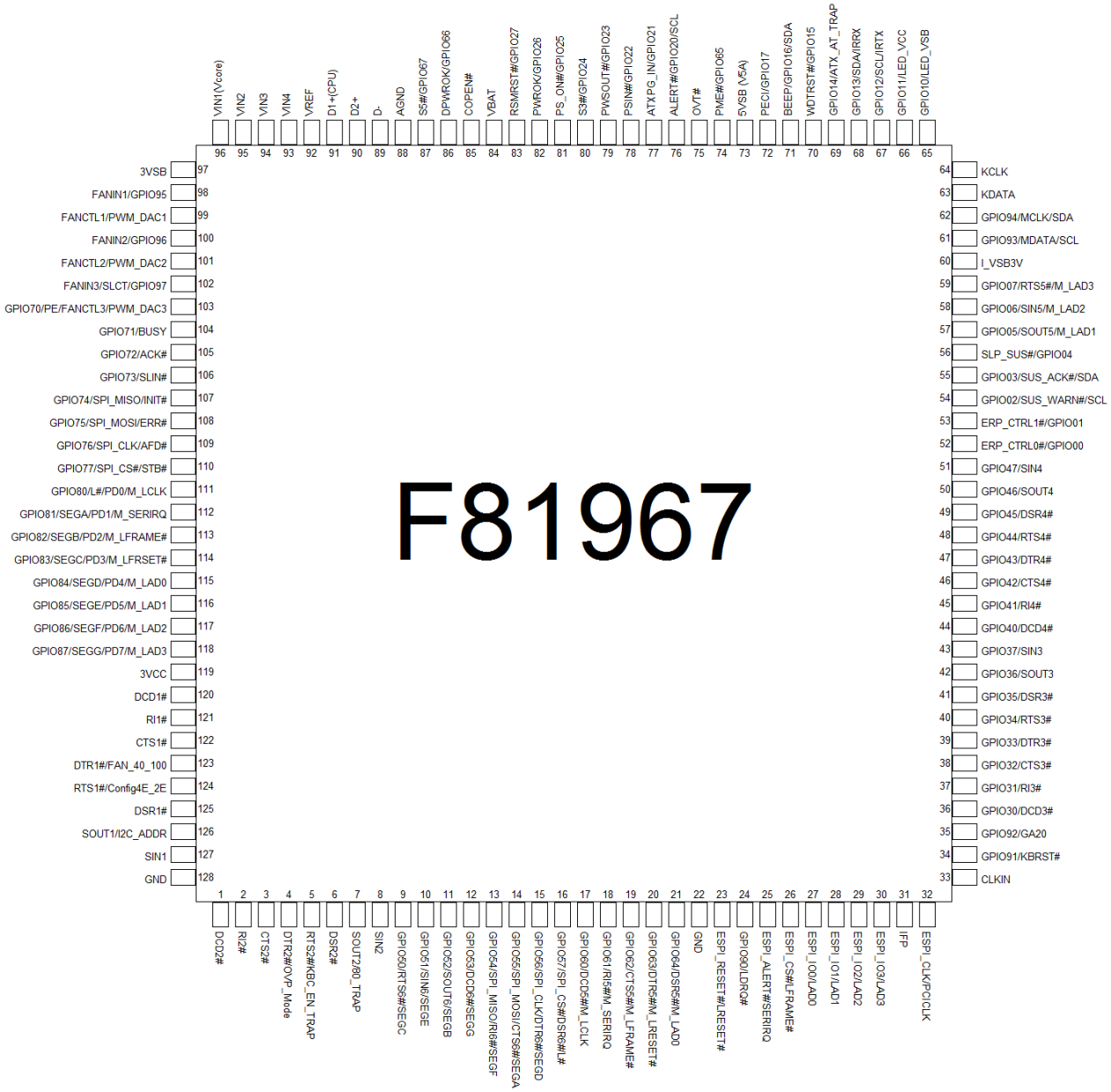


Figure2. F81966 pin configuration (14mm*14mm)

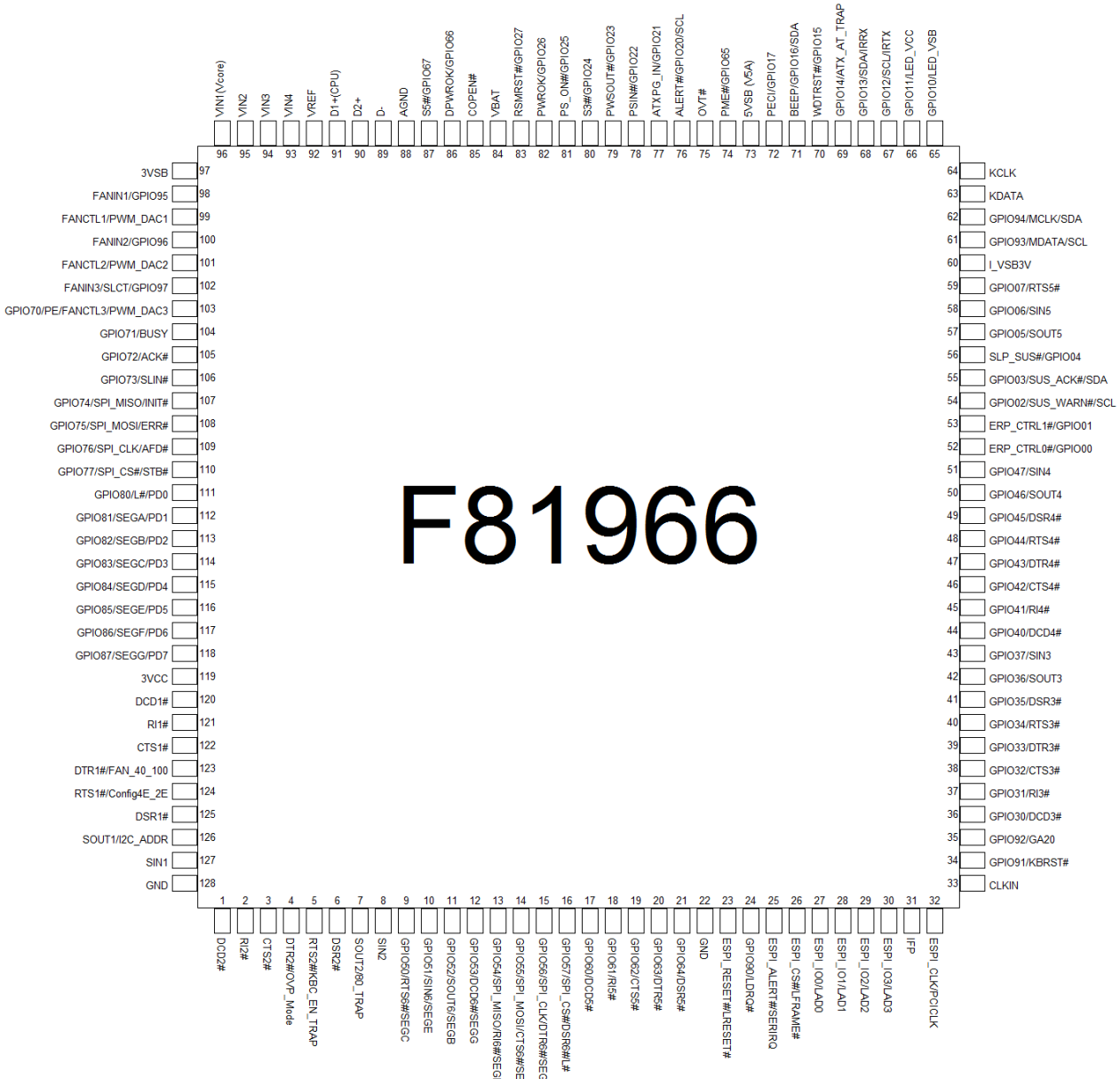


Figure3. F81964 pin configuration (14mm*14mm)

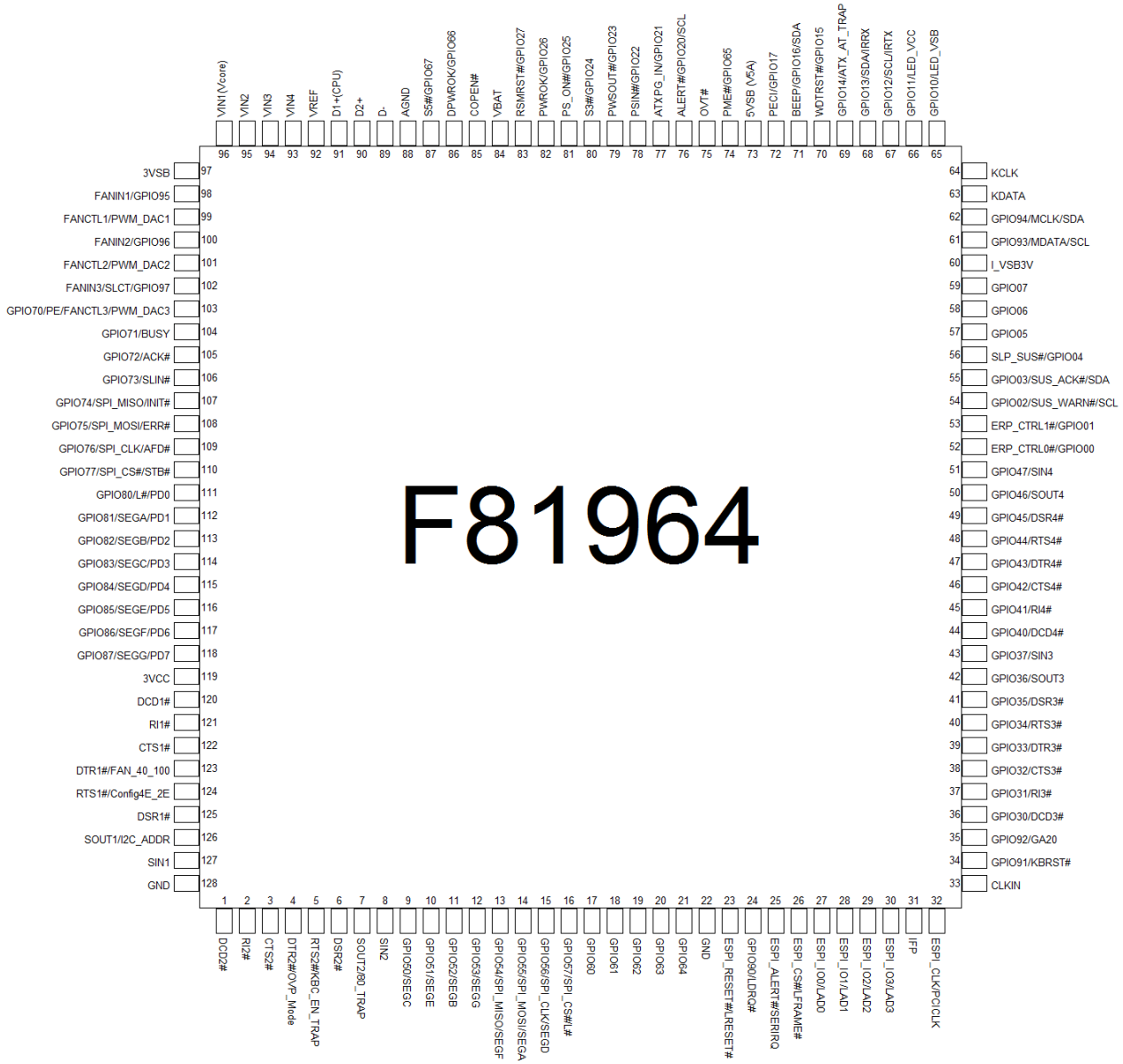
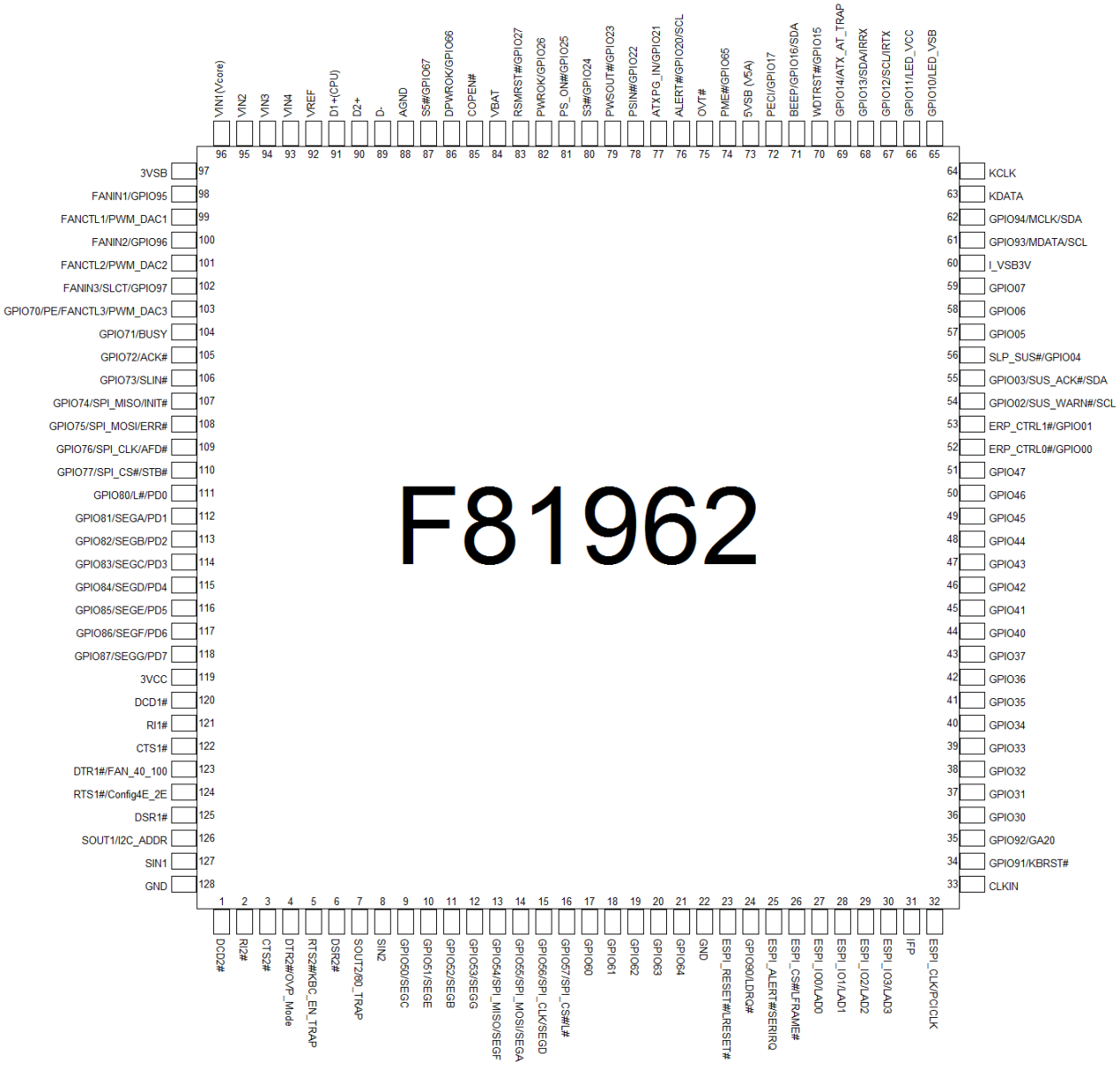


Figure4. F81962 pin configuration (14mm*14mm)



3.2 Pin Description

3.2.1 Power and Ground

F81967	F81966	F81964	F81962	Pin Name	Type	Description
119	119	119	119	3VCC	P	Power supply voltage input with 3.3V.
31	31	31	31	IFP	P	Interface 1.8V/3.3V power supply voltage input for LPC Interface 1.8V power supply voltage input for eSPI
60	60	60	60	I_VSB3V	P	3.3V internal standby power pin which regulates from 5VSB (V5A). This pin can be an output pin which could provide the small amount of the current at 5VSB (V5A) existence for extending the battery life.
84	84	84	84	VBAT	P	3.3V Battery Power.
73	73	73	73	5VSB (V5A)	P	5V standby power supply.
97	97	97	97	3VSB	P	Analog Power with 3.3V standby.
88	88	88	88	AGND	P	Analog GND. Analog ground used for all internal analog circuit, it must be grounded.
22	22	22	22	GND	P	Digital GND. Digital ground used for all internal digital circuit, it must be grounded.
128	128	128	128			

3.2.2 LPC & eSPI Clock

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
32	32	32	32	PCICLK	IN_{st}	IFP	PCI clock 10M Hz~33M Hz input.
33	33	33	33	CLKIN	IN_{st}	I_VSB3V	System clock input 24/48MHz (default 48MHz). CLKIN's clock would be programmable internally.

3.2.3 LPC Interface (Slave & Master) (Master only for F81967)

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
23	23	23	23	LRESET#	$IN_{st,lv}$	IFP	**LPC Reset Signal**. It can connect to PCIRST# signal on the host.
24	24	24	24	LDRQ#	O_{16}	IFP	Encoded DMA Request signal.
25	25	25	25	SERIRQ	I_{lv}/O_{lv}	IFP	LPC Serial IRQ input / Output.
26	26	26	26	LFRAME#	IN_{st}	IFP	Indicates start of a new cycle or termination of a broken cycle.
27-30	27-30	27-30	27-30	LAD[0:3]	I/O_{16st}	IFP	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
17, 111	-	-	-	M_LCLK	O_8	3VCC	Master LPC clock output 24MHz.
18, 112	-	-	-	M_SERIRQ	I/O_{16st}	3VCC	Master LPC Serial IRQ input / Output.
19, 113	-	-	-	M_LFRAME#	IN_{st}	3VCC	Master LPC frame: Indicates start of a new cycle or termination of a broken cycle.
20, 114	-	-	-	M_LRESET#	IN_{st}	3VCC	Master LPC Reset Signal. It can connect to PCIRST# signal on the host.
21, 115	-	-	-	M_LAD0	I/O_{12st}	3VCC	This signal line communicates address, control, and data information over the master LPC bus between a host and a peripheral.
57-59	-	-	-	M_LAD[1:3]	I/O_{12s}	I_VSB3V	
116-118				M_LAD[1:3]	I/O_{12s}	3VCC	

3.2.4 SPI and eSPI

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
13, 107	13, 107	13, 107	13, 107	SPI_MISO	$IN_{st,5v}$	3VCC	SPI master input, slave output
14, 108	14, 108	14, 108	14, 108	SPI_MOSI	$O_{16\text{-}5v}$	3VCC	SPI master output, slave input
15, 109	15, 109	15, 109	15, 109	SPI_CLK	$IN_{st,5v}$	3VCC	SPI clock.

16, 110	16, 110	16, 110	16, 110	SPI_CS#	$IN_{st,5v}$	3VCC	SPI chip select
23	23	23	23	ESPI_RESET#	$IN_{st,lv}$	IFP	eSPI Reset signal. Reset the eSPI interface for both master & slaves.
25	25	25	25	ESPI_ALERT#	$I/O_{16st,lv}$	IFP	eSPI Alert#: Used by eSPI slave to request service from eSPI master. This pin is optional for single master single slave configuration where I/O [1] can be used to signal the Alert event.
26	26	26	26	ESPI_CS#	$IN_{st,lv}$	IFP	eSPI Chip select#: driving chip select low selects a particular eSPI slave for the transaction.
27-30	27-30	27-30	27-30	ESPI_IO[0:3]	$I/O_{16st,lv}$	IFP	eSPI I/O: Bi directional input/output pins used to transfer data between master & slaves.
32	32	32	32	ESPI_CLK	$IN_{st,lv}$	IFP	eSPI clock input. The reference timing for all the serial input & output operations.

3.2.5 Parallel Port (LPT Port)

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
102	102	102	102	SLCT	$IN_{st,5v}$	3VCC	An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
103	103	103	103	PE	$IN_{st,5v}$	3VCC	An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
104	104	104	104	BUSY	$IN_{st,5v}$	3VCC	An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
105	105	105	105	ACK#	$IN_{st,5v}$	3VCC	An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this

							pin in ECP and EPP mode.
106	106	106	106	SLIN#	$I/OOD_{12st,5v}$	3VCC	Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
107	107	107	107	INIT#	$I/OOD_{12st,5v}$	3VCC	Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
108	108	108	108	ERR#	$IN_{st,5v}$	3VCC	An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
109	109	109	109	AFD#	$I/OOD_{12st,5v}$	3VCC	An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
110	110	110	110	STB#	$I/OOD_{12st,5v}$	3VCC	An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
111	111	111	111	PD0	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
112	112	112	112	PD1	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 1.
113	113	113	113	PD2	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 2.
114	114	114	114	PD3	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 3.
115	115	115	115	PD4	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 4.
116	116	116	116	PD5	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 5.
117	117	117	117	PD6	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 6.
118	118	118	118	PD7	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 7.

3.2.6 Hardware Monitor, I2C

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
54, 67, 76	54, 67, 76	54, 67, 76	54, 67, 76	SCL	$I_{IV}/OD_{12st, 5v}$	I_VSB3V	I2C Interface CLOCK pin. Clock output for AMD TSI, MXM, I2C & Intel PCH (IBX Peak).
61	61	61	61		$I_{IV}/OD_{16st, 5v}$		
55, 62, 68	55, 62, 68	55, 62, 68	55, 62, 68	SDA	$I_{IV}/OD_{12st, 5v}$	I_VSB3V	I2C Interface DATA pin. AMD TSI, MXM, I2C & Intel PCH (IBX Peak) data pin.
71	71	71	71		$I_{IV}/OD_{24st, 5v}$		
71	71	71	71	BEEP	$OD_{24t,5v}$	I_VSB3V	Beep pin. Program to GPIO; PME#; CLKOUT; LED_VSB; LED_VCC; WDTRST; ALERT# by register.
72	72	72	72	PECI	I_{Iv} /$O_{D8, S1}$	I_VSB3V	PECI interface pin.
75	75	75	75	OVT#	$OD_{12,5v}$	I_VSB3V	Over temperature signal output.
76	76	76	76	ALERT#	$OD_{12,5v}$	I_VSB3V	Alert a signal when temperature over limit setting.
85	85	85	85	COPEN#	$IN_{st,5v}$	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.
89	89	89	89	D-	AIN	3VSB	Analog GND for thermal diode/transistor temperature.
90	90	90	90	D2+	AIN	3VSB	Thermal diode/transistor temperature sensor input.
91	91	91	91	D1+(CPU)	AIN	3VSB	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
92	92	92	92	VREF	AOUT	3VSB	Voltage reference output.
93	93	93	93	VIN4	AIN	3VSB	Voltage Input 4.
94	94	94	94	VIN3	AIN	3VSB	Voltage Input 3. Support OVP & UVP function, and default is disable alarm mode.
95	95	95	95	VIN2	AIN	3VSB	Voltage Input 2. Support OVP & UVP function, and default is disable alarm mode.
96	96	96	96	VIN1 (Vcore)	AIN	3VSB	Voltage Input for Vcore.
98	98	98	98	FANIN1	$IN_{st,5v}$	3VCC	Fan 1 tachometer input.
99	99	99	99	FANCTL1	$OOD_{12,5v}$ AOUT	3VCC	Fan 1 control output. This pin provides PWM duty-cycle output or a DAC voltage output
100	100	100	100	FANIN2	$IN_{st,5v}$	3VCC	Fan 2 tachometer input.

101	101	101	101	FANCTL2	$OOD_{12,5v}$ AOUT	3VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a DAC voltage output (internal pull down 100k Ω , default).
102	102	102	102	FANIN3	$IN_{st,5v}$	3VCC	Fan 3 tachometer input.
103	103	103	103	FANCTL3	$OOD_{12,5v}$ AOUT	3VCC	Fan 3 control output. This pin provides PWM duty-cycle output or a DAC voltage output.

3.2.7 Keyboard and Mouse Controller (KBC)

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
34	34	34	34	KBRST#	$OD_{12,u10}$	I_VSB3V	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10KΩ.
35	35	35	35	GA20	$OD_{12,u10}$	I_VSB3V	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10KΩ.
61	61	61	61	MDATA	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Mouse Data.
62	62	62	62	MCLK	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Mouse Clock.
63	63	63	63	KDATA	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Keyboard Data.
64	64	64	64	KCLK	$I/OD_{16st,5V}$	I_VSB3V	PS/2 Keyboard Clock.

3.2.8 ACPI, ERP

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
52	52	52	52	ERP_CTRL0#	$OD_{12,5V}$	I_VSB3V	Standby power rail control pin 0. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
53	53	53	53	ERP_CTRL1#	$OD_{12,5V}$	I_VSB3V	Standby power rail control pin 1. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
54	54	54	54	SUS_WARN#	IN_{st}	I_VSB3V	This pin asserts low when the PCH is planning to enter the DSW power state. It can detect 5VDUAL level with delay setting supported. The delay time is 1ms~8S (default 4s)
55	55	55	55	SUS_ACK#	$OD_{12,5v}$	I_VSB3V	This pin must wait SUSWARN# signal for entering DSW power state.

56	56	56	56	SLP_SUS#	IN_{st}	I_VSB3V	This pin asserts low which comes from PCH to shut off suspend power rails externally to enhance power saving function.
65	65	65	65	LED_VSB	$OOD_{12,5V}$	I_VSB3V	Power LED for VSB. Program to GPIO; PME#; CLKOUT; Beep; LED_VCC; WDTRST; ALERT# by register.
66	66	66	66	LED_VCC	$OOD_{12,5V}$	I_VSB3V	Power LED for VCC. Program to GPIO; PME#; CLKOUT; Beep; LED_VSB; WDTRST; ALERT# by register.
70	70	70	70	WDTRST#	$OD_{12,5v}$	I_VSB3V	Watch dog timer signal output. Program to GPIO; PME#; CLKOUT; Beep; LED_VCC; LED_VSB; ALERT# by register.
74	74	74	74	PME#	$OD_{12,5v}$	I_VSB3V	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up. Program to GPIO; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
77	77	77	77	ATXPG_IN	$IN_{st,5v}$	I_VSB3V	ATX Power Good input. If do not use this pin, please pull up.
78	78	78	78	PSIN#	$IN_{st,5v}$	I_VSB3V	Main power switch button input.
79	79	79	79	PWSOUT#	$OD_{12,5V}$	I_VSB3V	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
80	80	80	80	S3#	$IN_{st,\ 5v}$	I_VSB3V	S3# Input is Main power on-off switch input.
81	81	81	81	PS_ON#	$OD_{12,5v}$	I_VSB3V	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
82	82	82	82	PWROK	$OD_{12,5V}$	VBAT	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V.
83	83	83	83	RSMRST#	$OD_{12,5V}$	VBAT	Resume Reset# function, It is power good signal of 3VSB, which is delayed 66ms as 3VSB arrives at 2.8V.
86	86	86	86	DPWROK	$OD_{12,5v}$	VBAT	It is power good signal of 5VSB which is delayed 66ms as 5VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.

87	87	87	87	S5#	$IN_{st\ 5v}$	I_VSB3V	S5# input. This pin companies with S3# to indicate the operating state from S0 to S3 and S4/S5 sleep states.

3.2.9 Serial Port 1 to 6 (UART 1 to 6)

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
1	1	1	1	DCD2#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
2	2	2	2	RI2#	$IN_{st,5v}$	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. Support wake up function.
3	3	3	3	CTS2#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
4	4	4	4	DTR2#	O_8	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
5	5	5	5	RTS2#	O_8	3VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
6	6	6	6	DSR2#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	7	7	7	SOUT2	O_8	3VCC	UART Serial Output. Used to transmit serial data out to the communication link.
8	8	8	8	SIN2	$IN_{st,5v}$	3VCC	UART Serial Input. Used to receive serial data through the communication link.
9	9	-	-	RTS6#	O_{16}	3VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
10	10	-	-	SIN6	$IN_{st,5v}$	3VCC	UART Serial Input. Used to receive serial data through the communication link.
11	11	-	-	SOUT6	O_{16}	3VCC	UART Serial Output. Used to transmit serial data out to the communication link.

12	12	-	-	DCD6#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
13	13	-	-	RI6#	$IN_{st,5v}$	3VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
14	14	-	-	CTS6#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
15	15	-	-	DTR6#	O_{16}	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
16	16	-	-	DSR6#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
17	17	-	-	DCD5#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
18	18	-	-	RI5#	$IN_{st,5v}$	3VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
19	19	-	-	CTS5#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
20	20	-	-	DTR5#	O_{16}	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
21	21	-	-	DSR5#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
36	36	36	-	DCD3#	$IN_{st,5v}$	I_VSB3V	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
37	37	37	-	RI3#	$IN_{st,,5v}$	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
38	38	38	-	CTS3#	$IN_{st,5v}$	I_VSB3V	Clear To Send is the modem control input.
39	39	39	-	DTR3#	O_8	I_VSB3V	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
40	40	40	-	RTS3#	O_8	I_VSB3V	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.

41	41	41	-	DSR3#	$IN_{st,5v}$	I_VSB3V	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
42	42	42	-	SOUT3	O_8	I_VSB3V	UART Serial Output. Used to transmit serial data out to the communication link.
43	43	43	-	SIN3	$IN_{st,5v}$	I_VSB3V	UART Serial Input. Used to receive serial data through the communication link.
44	44	44	-	DCD4#	$IN_{st,5v}$	I_VSB3V	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
45	45	45	-	RI4#	$IN_{st,5v}$	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
46	46	46	-	CTS4#	$IN_{st,5v}$	I_VSB3V	Clear To Send is the modem control input.
47	47	47	-	DTR4#	O_8	I_VSB3V	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
48	48	48	-	RTS4#	O_8	I_VSB3V	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
49	49	49	-	DSR4#	$IN_{st,5v}$	I_VSB3V	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
50	50	50	-	SOUT4	O_8	I_VSB3V	UART Serial Output. Used to transmit serial data out to the communication link.
51	51	51	-	SIN4	$IN_{st,5v}$	I_VSB3V	UART Serial Input. Used to receive serial data through the communication link.
57	57	-	-	SOUT5	O_8	I_VSB3V	UART Serial Output. Used to transmit serial data out to the communication link.
58	58	-	-	SIN5	$IN_{st,5v}$	I_VSB3V	UART Serial Input. Used to receive serial data through the communication link.
59	59	-	-	RTS5#	O_8	I_VSB3V	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
120	120	120	120	DCD1#	$IN_{st,5v}$	I_VSB3V	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
121	121	121	121	RI1#	$IN_{st,5v}$	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. Support wake up

							function.
122	122	122	122	CTS1#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
123	123	123	123	DTR1#	O_8	3VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
124	124	124	124	RTS1#	O_8	3VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
125	125	125	125	DSR1#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
126	126	126	126	SOUT1	O_8	3VCC	UART Serial Output. Used to transmit serial data out to the communication link.
127	127	127	127	SIN1	$IN_{st,5v}$	3VCC	UART Serial Input. Used to receive serial data through the communication link.

3.2.10 80 Port

※ 80 port's function is output from the printer's data bus in default.

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
9, 114	9, 114	9, 114	9, 114	SEGC	O_{18}	3VCC	SEGD for 7-segment display(Common Cathode). This function would be enabled by power on strapping pin 7 or programming the register.
10, 116	10, 116	10, 116	10, 116	SEGE	O_{18}	3VCC	
11, 113	11, 113	11, 113	11, 113	SEGB	O_{18}	3VCC	
12, 118	12, 118	12, 118	12, 118	SEGG	O_{18}	3VCC	
13, 117	13, 117	13, 117	13, 117	SEGF	O_{18}	3VCC	
14, 112	14, 112	14, 112	14, 112	SEGA	O_{18}	3VCC	
15, 115	15, 115	15, 115	15, 115	SEGD	O_{18}	3VCC	
16	16	16	16	L#	O_{16}	3VCC	L# for 7-segment display(Common Cathode). This function would be enabled by power on strapping pin 7 or programming the register.
111	111	111	111		O_{12}		

3.2.11 Infrared

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
67	67	67	67	IRTX	O_{12}	I_VSB3V	SIR Data Infrared Transmitter Output
68	68	68	68	IRRX	$IN_{st,\ 5V}$	I_VSB3V	SIR Data Infrared Receiver Input

Note: UART 6 can't be used if this function is valid.

3.2.12 General-Purpose I/O (GPIO)

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
9	9	9	9	GPIO50	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
10	10	10	10	GPIO51	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
11	11	11	11	GPIO52	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
12	12	12	12	GPIO53	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
13	13	13	13	GPIO54	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
14	14	14	14	GPIO55	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
15	15	15	15	GPIO56	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
16	16	16	16	GPIO57	$I/OOD_{14st, 5v}$	3VCC	General Purpose IO.
17	17	17	17	GPIO60	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
18	18	18	18	GPIO61	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
19	19	19	19	GPIO62	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
20	20	20	20	GPIO63	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
21	21	21	21	GPIO64	$I/OOD_{12st, 5v}$	3VCC	General Purpose IO.
24	24	24	24	GPIO90	$I/OOD_{12st, 5v}$	IFP	General Purpose IO.
34	34	34	34	GPIO91	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
35	35	35	35	GPIO92	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
36	36	36	36	GPIO30	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
37	37	37	37	GPIO31	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
38	38	38	38	GPIO32	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
39	39	39	39	GPIO33	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
40	40	40	40	GPIO34	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
41	41	41	41	GPIO35	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
42	42	42	42	GPIO36	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
43	43	43	43	GPIO37	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
44	44	44	44	GPIO40	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
45	45	45	45	GPIO41	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
46	46	46	46	GPIO42	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
47	47	47	47	GPIO43	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
48	48	48	48	GPIO44	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
49	49	49	49	GPIO45	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.
50	50	50	50	GPIO46	$I/OOD_{8st, 5v}$	I_VSB3V	General Purpose IO.

51	51	51	51	GPIO47	I/OOD$_{8st, 5v}$	I_VSB3V	General Purpose IO.
52	52	52	52	GPIO00	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
53	53	53	53	GPIO01	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
54	54	54	54	GPIO02	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
55	55	55	55	GPIO03	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
56	56	56	56	GPIO04	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
57	57	57	57	GPIO05	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
58	58	58	58	GPIO06	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
59	59	59	59	GPIO07	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
61	61	61	61	GPIO93	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
62	62	62	62	GPIO94	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
65	65	65	65	GPIO10	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
66	66	66	66	GPIO11	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
67	67	67	67	GPIO12	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
68	68	68	68	GPIO13	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
69	69	69	69	GPIO14	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
70	70	70	70	GPIO15	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
71	71	71	71	GPIO16	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
72	72	72	72	GPIO17	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO. Program to PME#; CLKOUT; Beep; LED_VCC; LED_VSB; WDTRST; ALERT# by register.
74	74	74	74	GPIO65	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
76	76	76	76	GPIO20	I/OOD$_{24st,5v}$	I_VSB3V	General purpose IO.

77	77	77	77	GPIO21	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
78	78	78	78	GPIO22	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
79	79	79	79	GPIO23	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
80	80	80	80	GPIO24	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
81	81	81	81	GPIO25	I/OOD$_{12st,5v}$	I_VSB3V	General purpose IO.
82	82	82	82	GPIO26	I/OD$_{12st,5v}$	I_VSB3V	General purpose IO.
83	83	83	83	GPIO27	I/OD$_{12st,5v}$	I_VSB3V	General purpose IO.
86	86	86	86	GPIO66	I/OD$_{12st,5v}$	VBAT	General purpose IO.
87	87	87	87	GPIO67	I/OD$_{12st,5v}$	VBAT	General purpose IO.
98	98	98	98	GPIO95	I/OD$_{12st,5v}$	3VCC	General purpose IO.
100	100	100	100	GPIO96	I/OD$_{12st,5v}$	3VCC	General purpose IO.
102	102	102	102	GPIO97	I/OD$_{12st,5v}$	3VCC	General purpose IO.
103	103	103	103	GPIO70	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
104	104	104	104	GPIO71	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
105	105	105	105	GPIO72	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
106	106	106	106	GPIO73	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
107	107	107	107	GPIO74	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
108	108	108	108	GPIO75	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
109	109	109	109	GPIO76	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
110	110	110	110	GPIO77	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
111	111	111	111	GPIO80	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
112	112	112	112	GPIO81	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
113	113	113	113	GPIO82	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
114	114	114	114	GPIO83	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
115	115	115	115	GPIO84	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
116	116	116	116	GPIO85	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
117	117	117	117	GPIO86	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.
118	118	118	118	GPIO87	I/OOD$_{12st,\ 5v}$	3VCC	General purpose IO.

3.2.13 Configuration Straps

F81967	F81966	F81964	F81962	Pin Name	Type	Pin PWR	Description
4	4	4	4	OVP_Mode	IN$_{t,u47,\ 5v}$	3VCC	1: Alert Mode. (default) 0: Force Mode
5	5	5	5	KBC_EN_TRAP	IN$_{t,u47,\ 5v}$	3VCC	Power on Strapping pin 1: Enable KBC after power on. (Default, internal pull high 47KΩ).

							0: Disable KBC after power on.
7	7	7	7	80_TRAP	$IN_{t,5v}$	3VCC	Power on strapping pin: 1(Default): Default 80-port enable (Internal pull high) 80 port decode output from LPT interface. It is also programmable 80 port decode output from UART 6 or printer's data bus where default if from printer's data bus. 0 : Disable 80-port function
69	69	69	69	ATX_AT_TRAP	$IN_{t,5v}$	I_VSB3V	Power on trapping: ATX emulates AT function 1: ATX mode (Default, internal pull high 47 KΩ). 0: AT mode.
99	99	99	99	PWM _DAC1	$IN_{st,5v}$	3VCC	Power on Strapping pin: 1: PWM mode. 0: Default is DAC mode for FANCTL1 (internal pull down 100 KΩ).
101	101	101	101	PWM _DAC2	$IN_{st,5v}$	3VCC	Power on Strapping pin: 1: PWM mode. 0: Default is DAC mode for FANCTL2 (internal pull down 100 KΩ).
103	103	103	103	PWM _DAC3	$IN_{st,5v}$	3VCC	Power on Strapping pin: 1: PWM mode. 0: Default is DAC mode for FANCTL3 (internal pull down 100 KΩ).
123	123	123	123	FAN_40_100	$IN_{t,u47,\ 5v}$	3VCC	Power on strapping pin: 1(Default): (Internal pull high 47 KΩ) Power on fan speed default duty is 40% (PWM). 0: Power on fan speed default duty is 100% (PWM).
124	124	124	124	Config4E_2E	$IN_{t,u47,\ 5v}$	3VCC	Power on strapping: 1(internal pull high 47KΩ,Default) Configuration register:4E/4F 0 Configuration register:2E/2F
126	126	126	126	I2C_ADDR	$IN_{t,u47,\ 5v}$	3VCC	1: I2C Slave Address is 7'h2E. (Default) 0: I2C Slave Address is 7'h2D.

4 Function Description

4.1 Parallel Port

The parallel port in F81962/F81964/F81966/F81967 support an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), and Extended Capabilities Parallel Port (ECP) mode. Refer to the configuration registers for more information on selecting the mode of operation. Below content is about the Parallel Port device register descriptions. All the registers are for software porting reference.

Base Address Setting

4.1.1 Parallel Port Data Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	DATA	R/W	LRESET#	00h	The output data to drive the parallel port data lines.

4.1.2 ECP Address FIFO Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	ECP_AFIFO	R/W	LRESET#	00h	Access only in ECP Parallel Port Mode and the ECP_MODE programmed in the Extended Control Register is 011. The data written to this register is placed in the FIFO and tagged as an Address/RLE. It is auto transmitted by the hardware. The operation is only defined for forward direction. It divide into two parts: Bit 7: 0: bits 6-0 are run length, indicating how many times the next byte to appear (0 = 1 time, 1 = 2 times, 2 = 3 times and so on). 1: bits 6-0 are ECP address. Bit 6-0: Address or RLE depends on bit 7.

4.1.3 Device Status Register — Base + 1

Bit	Name	R/W	Reset	Default	Description
7	BUSY_N	R	-	-	Inverted version of parallel port signal BUSY.
6	ACK_N	R	-	-	Version of parallel port signal ACK#.
5	PERROR	R	-	-	Version of parallel port signal PE.
4	SELECT	R	-	-	Version of parallel port signal SLCT.
3	ERR_N	R	-	-	Version of parallel port signal ERR#.
2-1	Reserved	R		11	Reserved. Return 11b when read.

0	TMOUT	R	LRESET#	-	This bit is valid only in EPP mode. Return 1 when in other modes. It indicates that a 10uS time out has occurred on the EPP bus. 0: no time out error. 1: time out error occurred, write 1 to clear.

4.1.4 Device Control Register — Base + 2

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	11	Reserved. Return 11b when read.
5	DIR	R/W	LRESET#	0	0: the parallel port is in output mode. 1: the parallel port is in input mode. It is auto reset to 1 when in SPP mode.
4	ACKIRQ_EN	R/W	LRESET#	0	Enable an interrupt at the rising edge of ACK#.
3	SLIN	R/W	LRESET#	0	Inverted and then drives the parallel port signal SLIN#. When read, the status of inverted SLIN# is return.
2	INIT_N	R/W	LRESET#	0	Drives the parallel port signal INIT#. When read, the status of INIT# is return.
1	AFD	R/W	LRESET#	0	Inverted and then drives the parallel port signal AFD#. When read, the status of inverted AFD# is return.
0	STB	R/W	LRESET#	0	Inverted and then drives the parallel port signal STB#. When read, the status of inverted STB# is return.

4.1.5 EPP Address Register — Base + 3

Bit	Name	R/W	Reset	Default	Description
7-0	EPP_ADDR	R/W	LRESET#	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Address Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Address Read protocol.

4.1.6 EPP Data Register — Base + 4 – Base + 7

Bit	Name	R/W	Reset	Default	Description
7-0	EPP_DATA	R/W	LRESET#	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Data Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Data Read protocol.

4.1.7 Parallel Port Data FIFO — Base + 400h

Bit	Name	R/W	Reset	Default	Description
7-0	C_FIFO	R/W	LRESET#	00h	Data written to this FIFO is auto transmitted by the hardware to the device by using standard parallel port protocol. It is only valid in ECP and the ECP_MODE is 010b.The operation is only for forward direction.

4.1.8 ECP Data FIFO — Base + 400h

Bit	Name	R/W	Reset	Default	Description
7-0	ECP_DFIFO	R/W	LRESET#	00h	Data written to this FIFO when DIR is 0 is auto transmitted by the hardware to the device by using ECP parallel port protocol. Data is auto read from device into the FIFO when DIR is 1 by the hardware by using ECP parallel port protocol. Read the FIFO will return the content to the system. It is only valid in ECP and the ECP_MODE is 011b.

4.1.9 ECP Test FIFO — Base + 400h

Bit	Name	R/W	Reset	Default	Description
7-0	T_FIFO	R/W	LRESET#	00h	Data may be read, written from system to the FIFO in any Direction. But no hardware handshake occurred on the parallel port lines. It could be used to test the empty, full and threshold of the FIFO. It is only valid in ECP and the ECP_MODE is 110b.G

4.1.10 ECP Configuration Register A — Base + 400h

Bit	Name	R/W	Reset	Default	Description
7	IRQ_MODE	R	LRESET#	0	0: interrupt is ISA pulse. 1: interrupt is ISA level. Only valid in ECP and ECP_MODE is 111b.
6-4	IMPID	R	LRESET#	001	000: the design is 16-bit implementation. 001: the design is 8-bit implementation (default). 010: the design is 32-bit implementation. 011-111: Reserved. Only valid in ECP and ECP_MODE is 111b.
3	Reserved	-	-	-	Reserved.
2	BYTETRAN_N	R	LRESET#	1	0: when transmitting there is 1 byte waiting in the transceiver that does not affect the FIFO full condition. 1: when transmitting the state of the full bit includes the byte being transmitted. Only valid in ECP and ECP_MODE is 111b.
1-0	Reserved	R	-	00	Return 00 when read. Only valid in ECP and ECP_MODE is 111b.

4.1.11 ECP Configuration Register B — Base + 401h

Bit	Name	R/W	Reset	Default	Description
7	COMP	R	LRESET#	0	0: only send uncompressed data. 1: compress data before sending. Only valid in ECP and ECP_MODE is 111b.
6	Reserved	R	-	1	Reserved. Return 1 when read. Only valid in ECP and ECP_MODE is 111b.
5-3	ECP_IRQ_CH	R	LRESET#	001	000: the interrupt selected with jumper. 001: select IRQ 7 (default). 010: select IRQ 9. 011: select IRQ 10. 100: select IRQ 11 101: select IRQ 14. 110: select IRQ 15. 111: select IRQ 5. Only valid in ECP and ECP_MODE is 111b.
2-0	ECP_DMA_CH	R	LRESET#	011	Return the DMA channel of ECP parallel port. Only valid in ECP and ECP_MODE is 111b.

4.1.12 Extended Control Register — Base + 402h

Bit	Name	R/W	Reset	Default	Description
7-5	ECP_MODE	R/W	LRESET#	000	000: SPP Mode. 001: PS/2 Parallel Port Mode. 010: Parallel Port Data FIFO Mode. 011: ECP Parallel Port Mode. 100: EPP Mode. 101: Reserved. 110: Test Mode. 111: Configuration Mode. Only valid in ECP.
4	ERRINTR_EN	R/W	LRESET#	0	0: disable the interrupt generated on the falling edge of ERR#. 1: enable the interrupt generated on the falling edge of ERR#.
3	DAMEN	R/W	LRESET#	0	0: disable DMA. 1: enable DMA. DMA starts when SERVICEINTR is 0.
2	SERVICEINTR	R/W	LRESET#	1	0: enable the following case of interrupt. DMAEN = 1: DMA mode. DMAEN = 0, DIR = 0: set to 1 whenever there are write Intr Threshold or more bytes are free in the FIFO. DMAEN = 0, DIR = 0: set to 1 whenever there are read Intr Threshold or more bytes are valid to be read in the FIFO.
1	FIFOFULL	R	LRESET#	0	0: The FIFO has at least 1 free byte. 1: The FIFO is completely full.

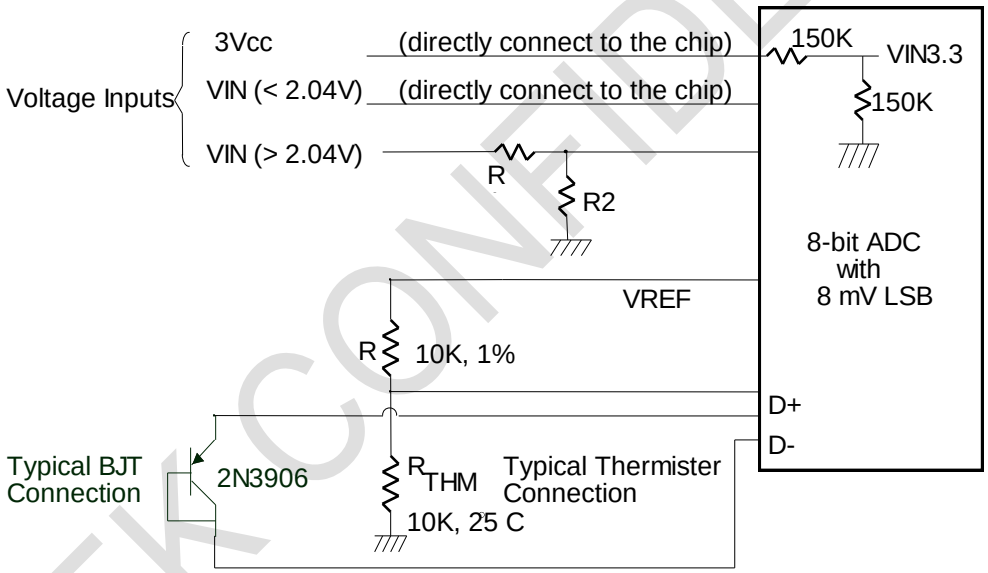
0	FIFOEMPTY	R	LRESET#	1	0: The FIFO contains at least 1 byte. 1: The FIFO is completely empty.

4.2 Hardware Monitor

4.2.1 Voltage

An 8-bit Analog to Digital Converter (ADC) has the 8mv LSB, and connected to external device pins (VIN1 ~ VIN4) and internal signal pins are 3VCC, 5VSB, VBAT and 3VSB. The maximum input voltage of the analog pin is 2.048V (256 steps × 8mV = 2.048V). Therefore the voltage under 2.048V (ex: 1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC is an exception for it is main power of F81962/F81964/F81966/F81967. Therefore 3VCC can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of F81962/F81964/F81966/F81967 and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150KΩ, so that the internal reduced voltage is half of +3.3V. Otherwise, there are two temperature sensor, a typical thermister and a typical bipolar junction transistor (BJT). Default Temperature Sensor is connected to a BJT.

Figure-1 Hardware monitor configuration



Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range, and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$

where V_{+12V} is the analog input voltage.

For example, we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance.

4.2.1.1 Over Voltage & Under Voltage Protection

F81962/F81964/F81966/F81967's voltage protection function could protect the damage from voltage spikes via over voltage & under voltage protection (OVP & UVP) function. Hardware strapping pin 4 default is alert mode (Default enable). Voltage protection function is enabled via setting the related register. When force mode occurs, the system would shut down and the

system cannot be re-booted at all. Only re-plugging the power code (cut off VSB) could re-activate or re-boot the system under force mode.

4.2.1.2 ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection. Therefore careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

4.2.2 Temperature

F81962/F81964/F81966/F81967 can monitor 2 types of remote temperature sensors in analog. They are thermistor and thermal Diode. These sensors can be measured from -60°C to 127°C for thermal diode & thermistor. Some popular sensors are recommended as bellow table.

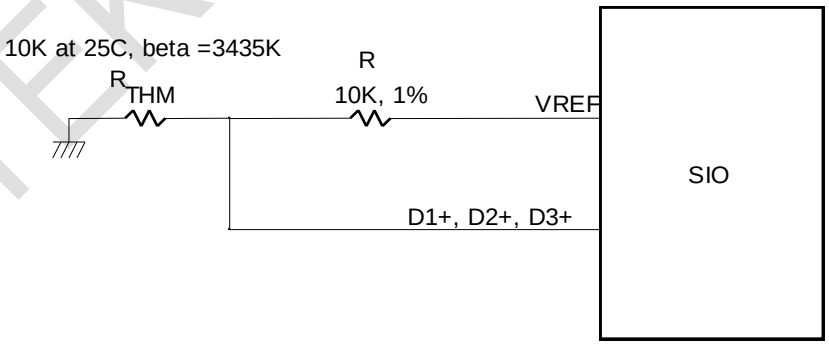
Table-1 Remote-sensor Transistor Manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

4.2.2.1 Thermistor

F81962/F81964/F81966/F81967 can connect 2 thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) ß value is 3435K (2) resistor value is 10K ohm at 25ºC. As below Figure, the thermistor is connected by a serial resistor with 10K ohm, then being connected to VREF.

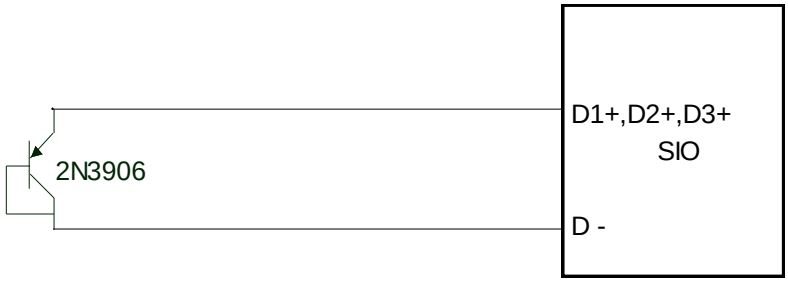
Figure -2 Monitor Temperature from Thermistor Configuration



4.2.2.2 Thermal Diode

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, F81962/F81964/F81966/F81967 is capable to these situations. The build-in reference table is for PNP 2N3906 transistor from Table 5-2. As below figure, the transistor is directly connected into temperature pins.

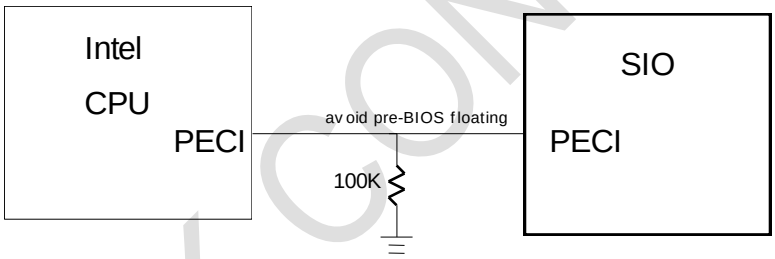
Figure 4-3 Monitor Temperature from Thermal Diode Configuration



4.2.2.3 Intel PECI

F81962/F81964/F81966/F81967 support Intel PECI1.1/PECI3.1 to read temperature from PECI signal. The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked on-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic '0' or login '1'. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple. The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information. F81962/F81964/F81966/F81967 can connect to CPU & read the temperature data from CPU directly. Then the fan control machine of F81962/F81964/F81966/F81967 can implement the fan to cool down CPU temperature. The application circuit is as below.

Figure -4 INTEL PECI Typical Application Method



The F81962/F81964/F81966/F81967 integrated most of PECI 3.1 commands for the future advantage application. More detail, please refer to the register descriptions.

Table -2 PECI 3.1 Command Support List

F81962/964/966/967Support	PECI 3.1 Command	PECI 1.0 Command	Status
V	Ping( )	Ping( )	
V	GetTemp( )	GetTemp( )	
V	GetDIB( )		
V	RdIAMSR( )		
-	WrIAMSR( )		
-	RdPCIConfigLocal( )		Not Available in Mobile/DT
-	WrPCIConfigLocal( )		Not Available in Mobile/DT
-	RdPCIConfig( )		Not Available in Mobile/DT

-	WrPCIConfig( )		Not Available in Mobile/DT
V	RdPkgConfig( )		
V	WrPkgConfig( )		

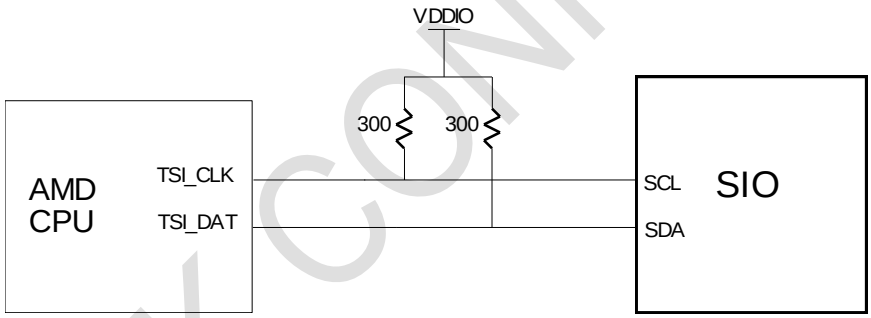
4.2.2.4 AMD TSI

The F81962/F81964/F81966/F81967 provide AMD Temperature Sensor Interface (TSI) interfaces for new generational CPU temperature sensing. In this interface, there are SIC and SID signals for temperature information reading from AMD CPU. The SIC signal is for clocking use, the other is for data transferring. More detail, please refer register description.

The TSI is a simple SMBUS master to communicate with AMD CPU or Intel CPU to getting the temperature of CPU. It supports byte sending, byte receiving, read/write byte, read/write block and quick command of SMBus protocol. When power on the hardware automatically fetch the temperature use the protocol per the specification of AMD/Intel. User can use the provided registers to control the SCL/SDA as a SMBus master. The SCL signal is for clocking use, the SDA is for data transferring.

F81962/F81964/F81966/F81967 provide SMBus block read/write compatible Platform Control Hub (PCH) EC SMBus protocol, and provides byte read/write protocol to read CPU and chipset thermal temperature information. For byte read/write protocol, F81962/F81964/F81966/F81967 supports 4-suit device address to read or write from device information. For block read/write, F81962/F81964/F81966/F81967 support 1 suits device address and maximum 17 byte count for read protocol to read from device information, and 4 byte count for write protocol to write information to device.

Figure 4-5 AMD TSI Typical Application Method



4.2.2.5 Temperature Interrupt Detection

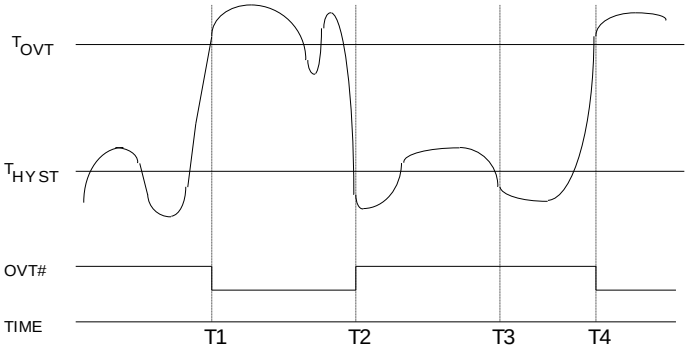
4.2.2.5.1 Over Temperature Signal (OVT#)

OVT# alert for temperature is shown as below figure. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

Figure -6 Temperature OVT# Signal

T_{OVT} : OVER Temperature Threshold

T_{HYST}: Hysteresis Temperature

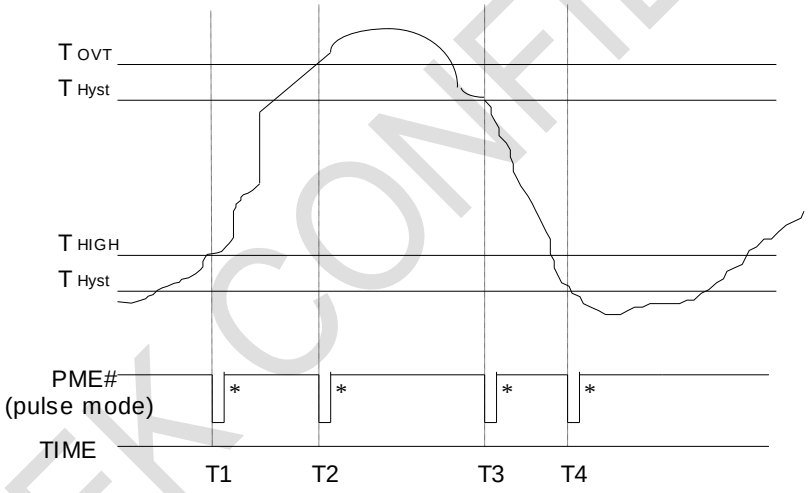


4.2.2.5.2 Power Management Event (PME#)

PME# interrupt for temperature is shown as below figure. Temperature exceeding high limit or going below hysteresis will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register.

Figure -7 Hysteresis mode illustrations

T_{OVT}: Over Temperature Threshold
T_{HYST}: Hysteresis Temperature
T_{HIGH}: High Limit Threshold



*Interrupt Reset when Interrupt Status Registers are written

4.2.3 Fan Control

4.2.3.1 Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$\text{Count} = \frac{1.5 \times 10^6}{\text{RPM}}$$

In other words, the fan speed counter (12 bit resolution) has been read from register, the fan speed can be evaluated by the following equation.

$$\text{RPM} = \frac{1.5 \times 10^6}{\text{Count}}$$

As for fan, it would be best to use 2 pulses (4 phases fan) tachometer output per round. So the parameter “Count” under 5 bit filter is 4096~64 and RPM is 366~23438 based on the above equation. If using 8 phases fan, RPM would be from 183~11719.

4.2.3.2 Fan Speed Control

These chips provide 2 fan speed control methods: 1. DAC FAN CONTROL 2. PWM DUTY CYCLE

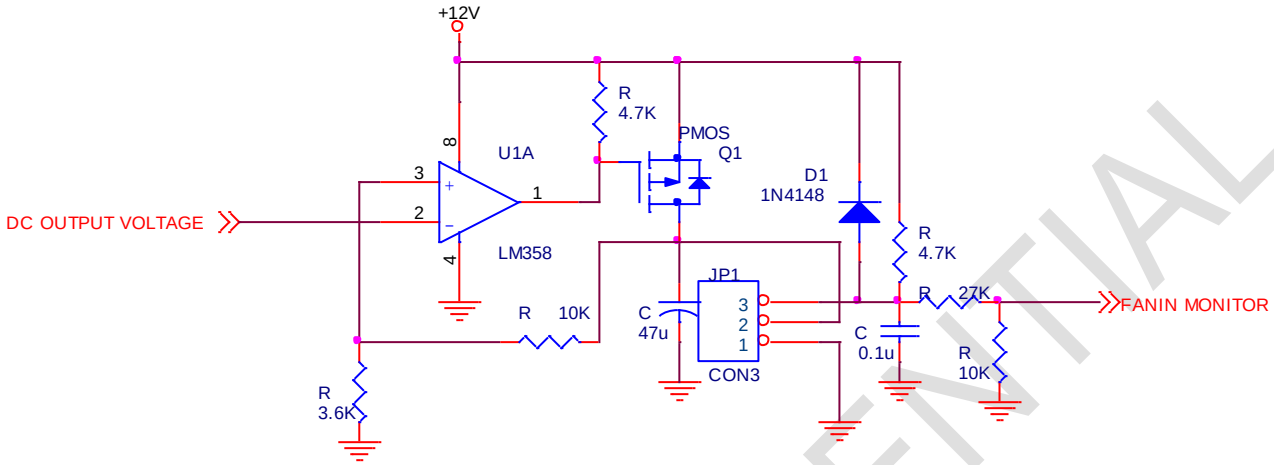
(1) DAC Fan Control

The range of DC output is 0~VCC, controlled by 8-bit register. 1 LSB is about 0.013V (VCC=3.3V). The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = \text{VCC} \times \frac{\text{Programmed 8bit Register Value}}{256}$$

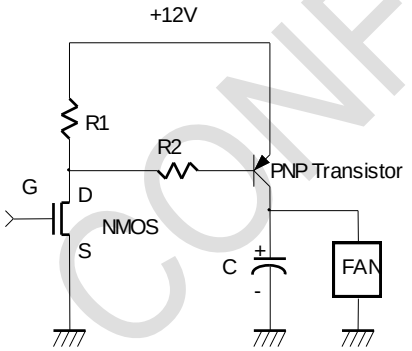
And the suggested application circuit for linear fan control would be:

Figure -8 Hysteresis mode illustrations



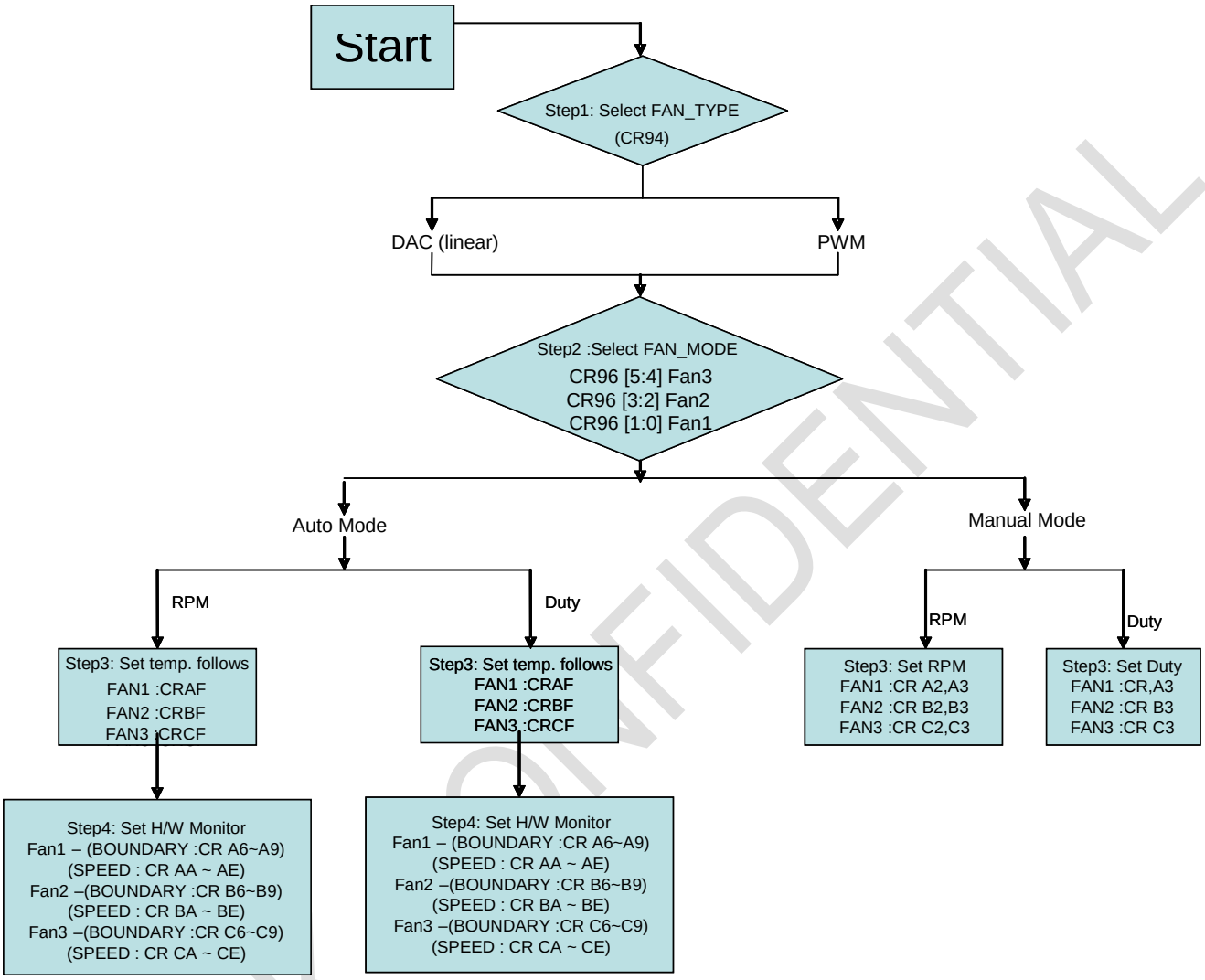
(2) PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.



$$Duty\_cycle(\%) = \frac{Programmed\ \ 8bit\ Register\ Value}{255} \times 100\%$$

Figure -9 Fan Control Mode Selection Flow



4.2.3.3 Fan Temperature Source

Each fan can be controlled by 8 kinds of temperature inputs: (1) T1 temperature (2) T2 temperature (3) T3 temperature (4) PECI temperature (5) 4 suits I2C master temperature.

Table Fan1 Type and Mode Selection

FAN 1	Related Register
FAN_PROG_SEL	Index 9Fh [7]
FAN Type Select	Index 94 [1:0]
FAN mode Select	Index 96 [1:0]
FAN count reading	Index A0h~A1h
FAN expect speed	Index A2h~A3h
FAN full speed count	Index A4h~A5h

FAN 1	Related Register
Boundary	Index A6h~A9h
Segment Speed	Index AAh~AEh
FAN1 Temperature Mapping	Index AFh
FAN1 Temperature Adjust Select	Index 96h[2:0]
FAN1 Temperature Adjust Up Rate	Index 95h[6:4]
FAN1 Temperature Adjust Down Rate	Index 95h[2:0]

Table Fan2 Type and Mode Selection

FAN 2	Related Register
FAN_PROG_SEL	Index 9Fh [7]
FAN Type Select	Index 94 [3:2]
FAN mode Select	Index 96 [3:2]
FAN count reading	Index B0h~B1h
FAN expect speed	Index B2h~B3h
FAN full speed count	Index B4h~B5h
Boundary	Index B6h~B9h
Segment Speed	Index BAh~BEh
FAN2 Temperature Mapping	Index BFh

Table Fan3 Type and Mode Selection

FAN 3	Related Register
FAN_PROG_SEL	Index 9Fh [7]
FAN Type Select	Index 94 [5:4]
FAN mode Select	Index 96 [5:4]
FAN count reading	Index C0h~C1h
FAN expect speed	Index C2h~C3h
FAN full speed count	Index C4h~C5h
Boundary	Index C6h~C9h
Segment Speed	Index CAh~CEh
FAN3 Temperature Mapping	Index CFh

4.2.3.4 Fan Speed Control mechanism

There are three modes for control fan speed and they are (1) Manual mode, and (2) Auto mode (Stage & Linear).

4.2.3.4.1 Manual mode

For manual mode, it generally acts as software fan speed control.

4.2.3.4.2 Auto mode

In auto mode, F81962/F81964/F81966/F81967 provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F81962/F81964/F81966/F81967 can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take FAN1 for example, the 4 temperature boundaries could be set from register 0xA6 to 0xA9 and the five intervals for fan speed control could be set from register 0xAA to 0xAE. And the hysteresis setting (0 ~ 15°C) could also be found in register 0x98.

The Manual Mode and Auto Mode could be selected by register 0x96h.

There are two kinds of auto mode: stage auto mode and linear auto mode. The “FAN1_INTERPOLATION_EN” in register 0xAFh is used for linear auto mode enable. The following examples explain the differences for stage auto mode and linear auto mode.

①. Fan Speed Auto Control Mode

In this mode, the fan keeps in a same speed for each temperature interval. And there are two types of fan speed setting:

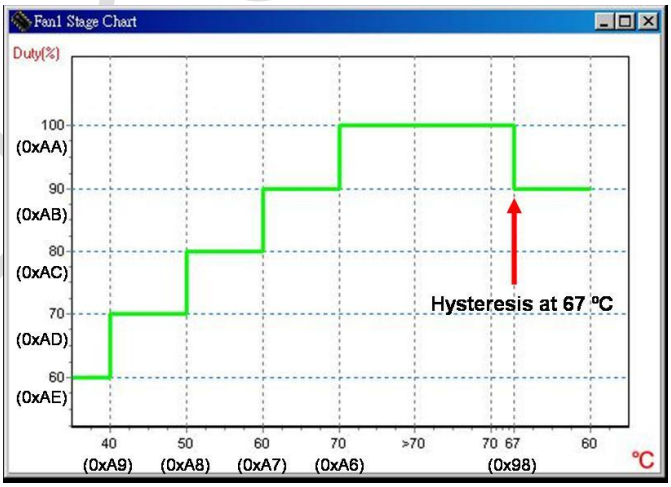
PWM Duty and RPM %.

i. Stage auto mode

✓ **Stage auto mode - PWM Duty**

Set the temperature limits as 70°C, 60°C, 50°C, 40°C and the duty as 100%, 90%, 80%, 70%, 60%

Figure -8 Stage mode fan control illustration-2



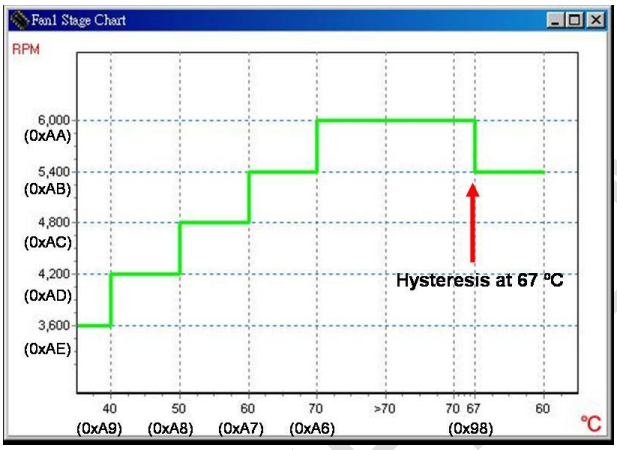
- Once the temperature is under 40°C, the lowest fan speed keeps in the 60% PWM duty.
- Once the temperature is over 40°C, 50°Cand 60°C, the fan speed will vary from 70%, 80% to 90% PWM duty and increasing with the temperature level.
- For the temperature higher than 70°C, the fan speed keeps in 100% PWM duty.
- If set the hysteresis is 3°C (default 4°C), once the temperature becomes lower than 67°C, the fan speed would

reduce to 90% PWM duty.

✓ **Stage auto mode - RPM%**

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 5,400 rpm, 4,800 rpm, 4,200 rpm, and 3,600 rpm (assume the Max Fan Speed is 6,000 rpm).

Figure -9 Stage mode fan control illustration-3



- Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,600 rpm (60% of full speed).
- Once the temperature is higher than 40°C, 50°C and 60°C, the fan speed will vary from 4,200 rpm to 5,400 rpm and increasing with the temperature level.
- For the temperature higher than 70°C, the fan speed keeps in the full speed 6,000 rpm.
- If the hysteresis is set as 3°C (default 4°C), once temperature gets lower than 67°C, the fan speed would reduce to 5,400 rpm.

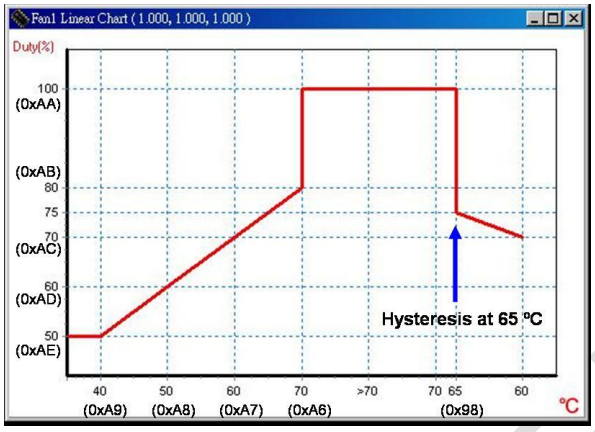
ii. Linear auto mode

F81962/F81964/F81966/F81967 also support linear auto mode. The fan speed would increase or decrease linearly with the temperature. There are also PWM Duty and RPM% modes for it.

✓ **Linear auto mode - PWM Duty**

Set the temperature as 70°C, 60°C, 50°C and 40°C and the duty is 100%, 80%, 70%, 60% and 50%.

Figure -10 Linear mode fan control illustration-1

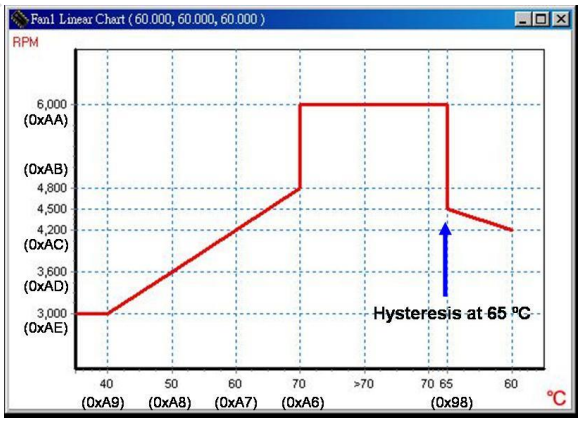


- Once the temperature is lower than 40°C, the lowest fan speed keeps in the 50% PWM duty
- Once the temperature becomes higher than 40°C, 50°C and 60°C, the fan speed will vary from 50% to 80% PWM duty linearly with the tempreature variation. The temp.-fan speed monitoring flash interval is 1sec.
- Once the temperature goes over 70°C, the fan speed will directly increase to 100% PWM duty (full speed).
- If set the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from 100% PWM duty and decrease linearly with the temperature.

✓ **Linear auto mode - RPM%**

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 4,800 rpm, 4,200 rpm, 3,600 rpm and 3,000 rpm (assume the Max Fan Speed is 6,000 rpm).

Figure -11 Linear mode fan control illustration-2



- Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,000 rpm (50% of full speed).
- Once the temperature is over 40°C, 50°C and 60°C, the fan speed will vary from 3,000 to 4,800 rpm almost linearly

with the temperature variation because the temp.-fan speed monitoring flash interval is 1sec.

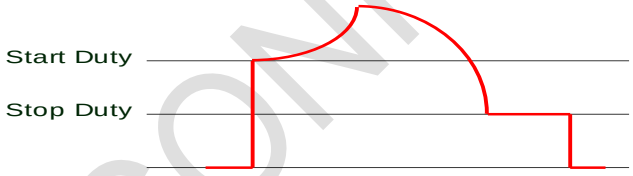
- Once the temperature goes over 70°C, the fan speed will directly increase to full speed 6,000 rpm.
- If the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from full speed and decrease linearly with the temperature.

4.2.3.5 PWMOUT Duty-cycle operating process

In both "Manual RPM" and "Temperature RPM" modes, the F81866A adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

1. When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.
2. When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.
3. If both (1) and (2) are not true,

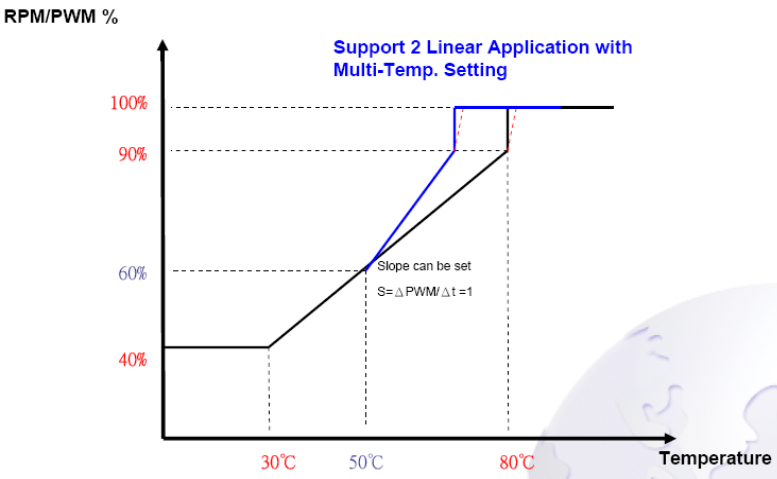
   When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, the F81866A will keep duty-cycle at 00h for 1.6 seconds. After that, the F81866A starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F81866A will ignore it.



4.2.3.6 Fan Speed Control with Multi-temperature

F81962/F81964/F81966/F81967 supports Multi-temperature for one fan control. This function works with linear auto mode can extend two linear slopes for one Fan control. As the graph below, this machine can support more silence fan control in low temperature environment and faster fan speed in high temperature segment. More detail setting please refers to the registers.

Figure 12 Support 2 Linear Application with Multi-Temperature Setting

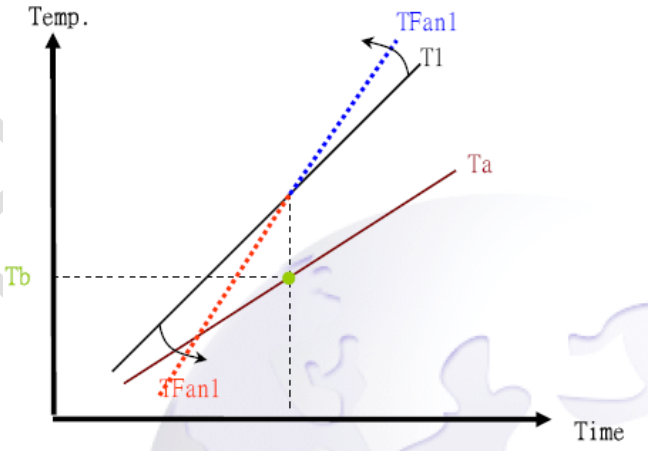


In the Figure below, TFan1 is the scaled temperature for fan1. T1 is the real temperature for the fan1 sensor. Ta is another temperature data which can be used for linearly scale up or scale down the fan1 speed curve. Tb would be the point which starts the temperature scaling. The slope for the temperature curve over and under Tb would be Ctup and Ctdn.

TFan1= T1 + (Ta-Tb)*Ctup

TFan1= T1 + (Ta-Tb)*Ctdn

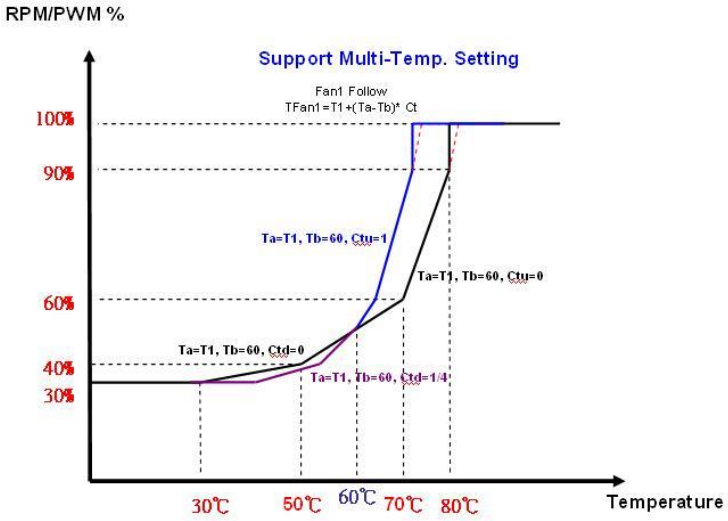
1. **Ctup**, **Ctdn** Can be Programmed to **1**, **½**, **¼**, **0**
2. **Ta** Can be Selected to the Same Temp. Source (Ex:T1)



In application, we can set the Ta as the 2nd sensor temperature and Tb as the temperature which starts the scaling. So if the 2nd sensor temperature Ta is higher or lower than Tb, the fan1 speed would be changed with it.

Figure -13 Example for the Multi-temperature

EX: Ta = T1, Tb = 60, Ctup = 1, Ctdn = 1/4

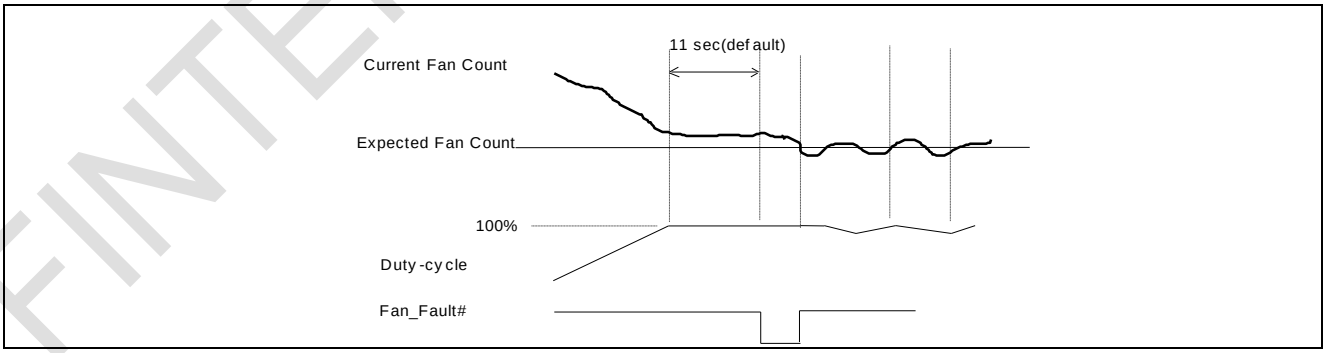


4.2.3.7 FAN_FAULT# (Internal Signal)

FAN_FAULT# will be asserted (Set in FAN Interrupt Status 91h[2:0], FAN Real Time Status 92h[2:0]. Related registers please refer to FAN PME# Enable 90h[2:0], FAN BEEP# Enable 93h[2:0]) when the fan speed doesn't meet the expected fan speed within a programmable period (default is 10 seconds, set in 9Fh[3:0]) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time.

Figure -14 FAN_FAULT# event



(2). After the period of detecting fan full speed, PWM_Duty > Min. Duty, fan count is still in 0xFFF.

4.3 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

4.3.1 Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60h. The keyboard controller uses the output buffer to send the code received from the keyboard and data bytes required by commands to the system.

4.3.2 Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60h or 64h. Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

4.3.3 Status Register

The status register is an 8-bit read-only register at I/O address 64h that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

4.3.4 Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><td>BIT</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Return 55h if self test succeeds</td></tr>
<tr><td>ABh</td><td>keyboard Interface Test
8’h00: indicate keyboard interface is ok.
8’h01: indicate keyboard clock is low.
8’h02: indicate keyboard clock is high
8’h03: indicate keyboard data is low
8’h04: indicate keyboard data is high</td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>C8h</td><td>Enable Keyboard/Mouse swap.</td></tr>
<tr><td>C9h</td><td>Disable Keyboard/Mouse swap.</td></tr>
<tr><td>CAh</td><td>Read the data written by CBh command.</td></tr>
<tr><td>CBh</td><td>Written a scratch data. This byte could be read by CAh command.</td></tr>
</table>

D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Low pulse on KBRST# about 6μS

KBC Command Description

4.3.5 PS/2 wakeup function

The KBC supports keyboard and mouse wakeup function. KBC will assert PME or PSOUT# signal. Those wakeup conditions are controlled by the configuration register.

4.4 General-Purpose Input / Output (GPIO) Ports

F81962/F81964/F81966/F81967 has 80 pins GPIO in total. All GPIO supports digit IO for Input/Output control, Output data control, input status and High/Low Level/Pulse, Open Drain/Push Pull function selection. The GPIO0x and GPIO1x support interrupt status. The GPIO0x, GPIO1x, GPIO5x, and GPIO8x have different SIRQ channels. Please see follows section for GPIO access methods and status:

4.4.1 GPIO Access Method

There are nine sets of GPIO which can be accessed by three ways as below:

1. Configuration register port: Use 0x4E/0x4F (or 0x2E/0x2F) port with logic device number 0x06. Please refer to configuration register for detail.
2. Index/Data port: The index port is base address + 0 and data port is base address + 1. To access the GPIO register, user should first write index to index port and then read/write from/to data port. The index for each register is same as the definition in configuration register.
3. Digital I/O: This way could access GPIO data register only. It is used for quickly control the GPIO pins. The register for each address is as below table:

GPIO Digital I/O Registers									
Offset	**Register Name**	**Default Value**							
		MSB							**LSB**
0h	Index Port	1	1	1	1	1	1	1	1
1h	Data Port	-	-	-	-	-	-	-	-
2h	GPIO8 Data Port	-	-	-	-	-	-	-	-
3h	GPIO7 Data Port	-	-	-	-	-	-	-	-
4h	GPIO6 Data Port	-	-	-	-	-	-	-	-
5h	GPIO5 Data Port	-	-	-	-	-	-	-	-
6h	GPIO0 Data Port	-	-	-	-	-	-	-	-
7h	GPIO1 Data Port	-	-	-	-	-	-	-	-
8h*	GPIO2 Data Port	-	-	-	-	-	-	-	-
9h*	GPIO3 Data Port	-	-	-	-	-	-	-	-
Ah*	GPIO4 Data Port	-	-	-	-	-	-	-	-
Bh*	GPIO9 Data Port	-	-	-	-	-	-	-	-
E-Fh*	Reserved	-	-	-	-	-	-	-	-

*Available when GPIO_DEC_RANGE is set “1” (Configuration register index 0x27, bit 5)

GPIO8 Data Port — Index 02h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO8_DATA	R/W	LRESET#	-	GPIO8 Data Control Write data to this byte will change the value of GPIO80_ DATA ~ GPIO87_ DATA in configuration register as writing data to index 0x89. Read data from this byte will read the pin status of GPIO80_ST ~ GPIO87_ST as the value in index 0x8A

GPIO7 Data Port — Index 03h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO7_DATA	R/W	LRESET#	-	GPIO7 Data Control Write data to this byte will change the value of GPIO70_ DATA ~ GPIO77_ DATA in configuration register as writing data to index 0x81. Read data from this byte will read the pin status of GPIO70_ST ~ GPIO77_ST as the value in index 0x82

GPIO6 Data Port — Index 04h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO6_DATA	R/W	LRESET#	-	GPIO6 Data Control Write data to this byte will change the value of GPIO60_ DATA ~ GPIO67_ DATA in configuration register as writing data to index 0x91. Read data from this byte will read the pin status of GPIO60_ST ~ GPIO67_ST as the value in index 0x92

GPIO5 Data Port — Index 05h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO5_DATA	R/W	LRESET#	-	GPIO5 Data Control Write data to this byte will change the value of GPIO50_ DATA ~ GPIO57_ DATA in configuration register as writing data to index 0xA1. Read data from this byte will read the pin status of GPIO50_ST ~ GPIO57_ST as the value in index 0xA2

GPIO0 Data Port — Index 06h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO0_DATA	R/W	5VSB	-	GPIO0 Data Control Write data to this byte will change the value of GPIO00_ DATA ~ GPIO07_ DATA in configuration register as writing data to index 0xF1. Read data from this byte will read the pin status of GPIO00_ST ~ GPIO07_ST as the value in index 0xF2

GPIO1 Data Port — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO1_DATA	R/W	5VSB	-	GPIO1 Data Control Write data to this byte will change the value of GPIO10_ DATA ~ GPIO17_ DATA in configuration register as writing data to index 0xE1. Read data from this byte will read the pin status of GPIO10_ST ~ GPIO17_ST as the value in index 0xE2

***GPIO2 Data Port — Index 08h**

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO2_DATA	R/W	5VSB	-	GPIO2 Data Control, this byte is available when GPIO_DEC_RANGE is set. Write data to this byte will change the value of GPIO20_ DATA ~ GPIO27_ DATA in configuration register as writing data to index 0xD1. Read data from this byte will read the pin status of GPIO20_ST ~ GPIO27_ST as the value in index 0xD2

***GPIO3 Data Port — Index 09h**

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO3_DATA	R/W	LRESET#	-	GPIO3 Data Control, this byte is available when GPIO_DEC_RANGE is set. Write data to this byte will change the value of GPIO30_ DATA ~ GPIO37_ DATA in configuration register as writing data to index 0xC1. Read data from this byte will read the pin status of GPIO30_ST ~ GPIO37_ST as the value in index 0xC2

GPIO4 Data Port — Index 0Ah

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO4_DATA	R/W	LRESET#	-	GPIO4 Data Control, this byte is available when GPIO_DEC_RANGE is set. Write data to this byte will change the value of GPIO40_DATA ~ GPIO47_DATA in configuration register as writing data to index 0xB1. Read data from this byte will read the pin status of GPIO40_ST ~ GPIO47_ST as the value in index 0xB2

***GPIO9 Data Port — Index 0Bh**

Bit	Name	R/W	Reset	Default	Description
7-0	GPIO9_DATA	R/W	LRESET#	-	GPIO4 Data Control, this byte is available when GPIO_DEC_RANGE is set. Write data to this byte will change the value of GPIO90_VAL ~ GPIO97_VAL in configuration register as writing data to index 0x99. Read data from this byte will read the pin status of GPIO90_IN ~ GPIO97_IN as the value in index 0x9A.

4.4.2 GPIO status

- Z means high impendence.
- If the external circuit is pull high then the pin status is "H"; else if the external circuit is pull low then the pin status is "L".
- User define means by programming the configure register.

4.4.2.1 GPIO0x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
52	GPIO00	L	user define	user define	user define	5VSB	5VSB	5VSB
53	GPIO01	L	user define	user define	user define	5VSB	5VSB	5VSB
54	GPIO02	Z	user define	user define	user define	5VSB	5VSB	5VSB
55	GPIO03	L	user define	user define	user define	5VSB	5VSB	5VSB
56	GPIO04	Z	user define	user define	user define	5VSB	5VSB	5VSB
57	GPIO05	Z	user define	user define	user define	5VSB	5VSB	5VSB
58	GPIO06	Z	user define	user define	user define	5VSB	5VSB	5VSB
59	GPIO07	Z	user define	user define	user define	5VSB	5VSB	5VSB

4.4.2.2 GPIO1x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
65	GPIO10	Z	user define	user define	user define	5VSB	5VSB	5VSB
66	GPIO11	Z	user define	user define	user define	5VSB	5VSB	5VSB
67	GPIO12	Z	user define	user define	user define	5VSB	5VSB	5VSB
68	GPIO13	Z	user define	user define	user define	5VSB	5VSB	5VSB
69	GPIO14	Z	user define	user define	user define	5VSB	5VSB	5VSB
70	GPIO15	Z	user define	user define	user define	5VSB	5VSB	5VSB
71	GPIO16	Z	user define	user define	user define	5VSB	5VSB	5VSB
72	GPIO17	Z	user define	user define	user define	5VSB	5VSB	5VSB

4.4.2.3 GPIO2x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
76	GPIO20	Z	user define	user define	user define	VBAT	VBAT	5VSB
77	GPIO21	Z	user define	user define	user define	VBAT	VBAT	5VSB
78	GPIO22	Z	user define	user define	user define	VBAT	VBAT	5VSB
79	GPIO23	Z	user define	user define	user define	VBAT	VBAT	5VSB
80	GPIO24	Z	user define	user define	user define	VBAT	VBAT	5VSB
81	GPIO25	Z	user define	user define	user define	VBAT	VBAT	5VSB
82	GPIO26	L	user define	user define	user define	VBAT	VBAT	5VSB
83	GPIO27	L	user define	user define	user define	VBAT	VBAT	5VSB

4.4.2.4 GPIO3x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
36	GPIO30	Z	user define	Z	Z	5VSB	5VSB	5VSB
37	GPIO31	Z	user define	Z	Z	5VSB	5VSB	5VSB
38	GPIO32	Z	user define	Z	Z	5VSB	5VSB	5VSB
39	GPIO33	Z	user define	Z	Z	5VSB	5VSB	5VSB
40	GPIO34	Z	user define	Z	Z	5VSB	5VSB	5VSB
41	GPIO35	Z	user define	Z	Z	5VSB	5VSB	5VSB
42	GPIO36	Z	user define	Z	Z	5VSB	5VSB	5VSB
43	GPIO37	Z	user define	Z	Z	5VSB	5VSB	5VSB

4.4.2.5 GPIO4x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
44	GPIO40	Z	user define	Z	Z	5VSB	5VSB	5VSB
45	GPIO41	Z	user define	Z	Z	5VSB	5VSB	5VSB
46	GPIO42	Z	user define	Z	Z	5VSB	5VSB	5VSB
47	GPIO43	Z	user define	Z	Z	5VSB	5VSB	5VSB
48	GPIO44	Z	user define	Z	Z	5VSB	5VSB	5VSB
49	GPIO45	Z	user define	Z	Z	5VSB	5VSB	5VSB
50	GPIO46	Z	user define	Z	Z	5VSB	5VSB	5VSB
51	GPIO47	Z	user define	Z	Z	5VSB	5VSB	5VSB

4.4.2.6 GPIO5x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
9	GPIO50	Z	user define	Z	Z	5VSB	3VCC	3VCC
10	GPIO51	Z	user define	Z	Z	5VSB	3VCC	3VCC
11	GPIO52	Z	user define	Z	Z	5VSB	3VCC	3VCC
12	GPIO53	Z	user define	Z	Z	5VSB	3VCC	3VCC
13	GPIO54	Z	user define	Z	Z	5VSB	3VCC	3VCC
14	GPIO55	Z	user define	Z	Z	5VSB	3VCC	3VCC
15	GPIO56	Z	user define	Z	Z	5VSB	3VCC	3VCC
16	GPIO57	Z	user define	Z	Z	5VSB	3VCC	3VCC

4.4.2.7 GPIO6x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
17	GPIO60	Z	user define	Z	Z	5VSB	3VCC	3VCC
18	GPIO61	Z	user define	Z	Z	5VSB	3VCC	3VCC
19	GPIO62	Z	user define	Z	Z	5VSB	3VCC	3VCC
20	GPIO63	Z	user define	Z	Z	5VSB	3VCC	3VCC
21	GPIO64	Z	user define	Z	Z	5VSB	3VCC	3VCC
74	GPIO65	Z	user define	Z	Z	5VSB	3VCC	5VSB
86	GPIO66	Z	user define	Z	Z	5VSB	3VCC	VBAT
87	GPIO67	Z	user define	Z	Z	5VSB	3VCC	VBAT

** GPIO66 and GPIO67 have no push pull function.*

4.4.2.8 GPIO7x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
103	GPIO70	Z	user define	Z	Z	5VSB	3VCC	3VCC
104	GPIO71	Z	user define	Z	Z	5VSB	3VCC	3VCC
105	GPIO72	Z	user define	Z	Z	5VSB	3VCC	3VCC
106	GPIO73	Z	user define	Z	Z	5VSB	3VCC	3VCC
107	GPIO74	Z	user define	Z	Z	5VSB	3VCC	3VCC
108	GPIO75	Z	user define	Z	Z	5VSB	3VCC	3VCC
109	GPIO76	Z	user define	Z	Z	5VSB	3VCC	3VCC
110	GPIO77	Z	user define	Z	Z	5VSB	3VCC	3VCC

4.4.2.9 GPIO8x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
111	GPIO80	Z	user define	Z	Z	5VSB	3VCC	3VCC
112	GPIO81	Z	user define	Z	Z	5VSB	3VCC	3VCC
113	GPIO82	Z	user define	Z	Z	5VSB	3VCC	3VCC
114	GPIO83	Z	user define	Z	Z	5VSB	3VCC	3VCC
115	GPIO84	Z	user define	Z	Z	5VSB	3VCC	3VCC
116	GPIO85	Z	user define	Z	Z	5VSB	3VCC	3VCC
117	GPIO86	Z	user define	Z	Z	5VSB	3VCC	3VCC
118	GPIO87	Z	user define	Z	Z	5VSB	3VCC	3VCC

4.4.2.10 GPIO9x

Pin	Name	PIN STATUS				Register Power Well	Register Reset Signal	Pin Power Well
		G3 -> S5	S0	S3	S5			
24	GPIO90	Z	User define	Z	Z	5VA	3VCC	IFP
34	GPIO91	Z	User define	Z	Z	5VA	3VCC	3VCC
35	GPIO92	Z	User define	Z	Z	5VA	3VCC	3VCC
61	GPIO93	Z	User define	Z	Z	5VA	3VCC	5VA
62	GPIO94	Z	User define	Z	Z	5VA	3VCC	5VA
98	GPIO95	Z	User define	Z	Z	5VA	3VCC	3VCC
100	GPIO96	Z	User define	Z	Z	5VA	3VCC	3VCC
102	GPIO97	Z	User define	Z	Z	5VA	3VCC	3VCC

4.5 Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal depends on register setting. The time unit has two ways from 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Others, please refer the device register description as below.

Base Address Setting

4.5.1 Watchdog Timer Configuration Register 1 — base address + 05h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	--	--	--	Reserved
6	WDTMOUT_STS	R/W	5VSB	0	If watchdog timeout event occurred, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	5VSB	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	5VSB	0	Select output mode (0: level, 1: pulse) of WDTRST# by setting this bit.
3	WD_UNIT	R/W	5VSB	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	5VSB	0	Select output polarity of WDTRST# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	5VSB	00b	Select output pulse width of WDTRST# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

4.5.2 Watchdog Timer Configuration Register 2 — base address + 06h

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME	R/W	5VSB	0h	Time of watchdog timer

4.5.3 Watchdog PME Control Register — base address + 0Ah

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME	R	5VSB	--	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	5VSB	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5	Reserved	--	--	--	Reserved.
4	WDT_CLK_SEL	R/W	5VSB	1	WDT clock source select 0: Internal clock. (No CLKIN is needed) 1: External clock derived by CLKIN. (more accurate)

3-1	Reserved	--	--	--	Reserved.
0	WDOUT_EN	R/W	5VSB	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.

4.6 ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to the full-power state, the disk is slower than the memory and the computer takes longer time to come back to the full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

ACPI includes three sub items as below:

1. Power Control (Include wake up via sleep state, wake up stage detection, AC loss & resume control methods)
2. Intel Power Saving Function (Deep Sleep Well, DSW: see next section for the detail)
3. EU Power Saving Function (EUP/ERP Command Lot 6.0: see next section for the detail)

Where item 2 & 3 could be coexisted via ERP_CTRL0# (follow SLP_SUS#) & ERP_CTRL1# (After the system enters S3 1.024s & S5 6.4s, EUP/ERP mode could be achieved).

Before entering into the main section, let's check out the related hardware control signal first.

Control Signal	Power On/Off Control (AC Resume)	Power Management Event	Wake up	Intel DSW Hand Shaking	EUP/ERP Control
RSMRST#	◇				
S3#	◇				
S5#	◇				
PSIN#	◇				
PWSOUT#	◇		☆★		
ATXPG_IN	◇				
PS_ON#	◇				
PWROK	◇				
PME#		◇	☆★		
PS/2 KB/MS			☆★		
RI1#/RI2#			☆★		
GPIO0x/GPIO1x			☆★		
SLP_SUS#				◇	
SUS_ACK#				◇	
SUS_WARN#				◇	
ERP_CTRL0#				◇	◇
ERP_CTRL1#					◇

◇: Supported
★: Wake up via ERP
☆: Wake up via System

4.6.1 Power Control

Wake up by PME#	Index 0x2D		CR0A Index 0xE0, 0xE8	CR0A Index 0xF0~0xF3
Normal Sleep State	◇			◇
EUP/ERP	◇		◇	
Wake up by PWSOUT#	**Index 0x2D**	**CR 0A Index 0x30**	**CR0A Index 0xE0, 0xE8**	**CR0A Index 0xF4**
Normal Sleep State	◇	◇		◇
EUP/ERP	◇	◇	◇	

4.6.1.1 Wake Up Via Sleep State

When the system is at the normal sleep state (S3, S4, S5) or deep sleep (G3') state, F81962/F81964/F81966/F81967 could wake up via PWSOUT# & PME#. See below for the related registers:

◇: Supported

4.6.1.2 Wake Up Stage Detection

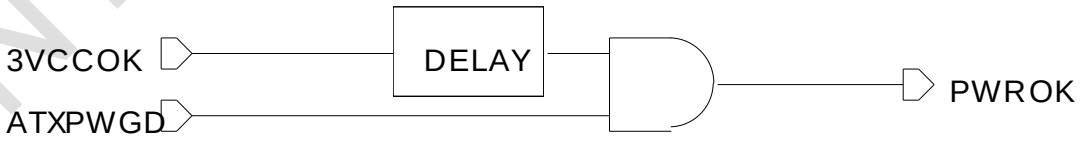
F81962/F81964/F81966/F81967 is counted on the chipset SLP_S3#, SLP_S4#/SLP_S5# stage, to decide the wake up stage as below:

ACPI Stage	SLP_S3#	SLP_S4# /SLP_S5#
S0	H	H
S3	L	H
S5	L	L

H: High; L: Low

Power saving mode would be activated via CR0A index E0 bit 7.

4.6.1.3 PWROK Signals



PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed via register (100ms ~ 400ms).

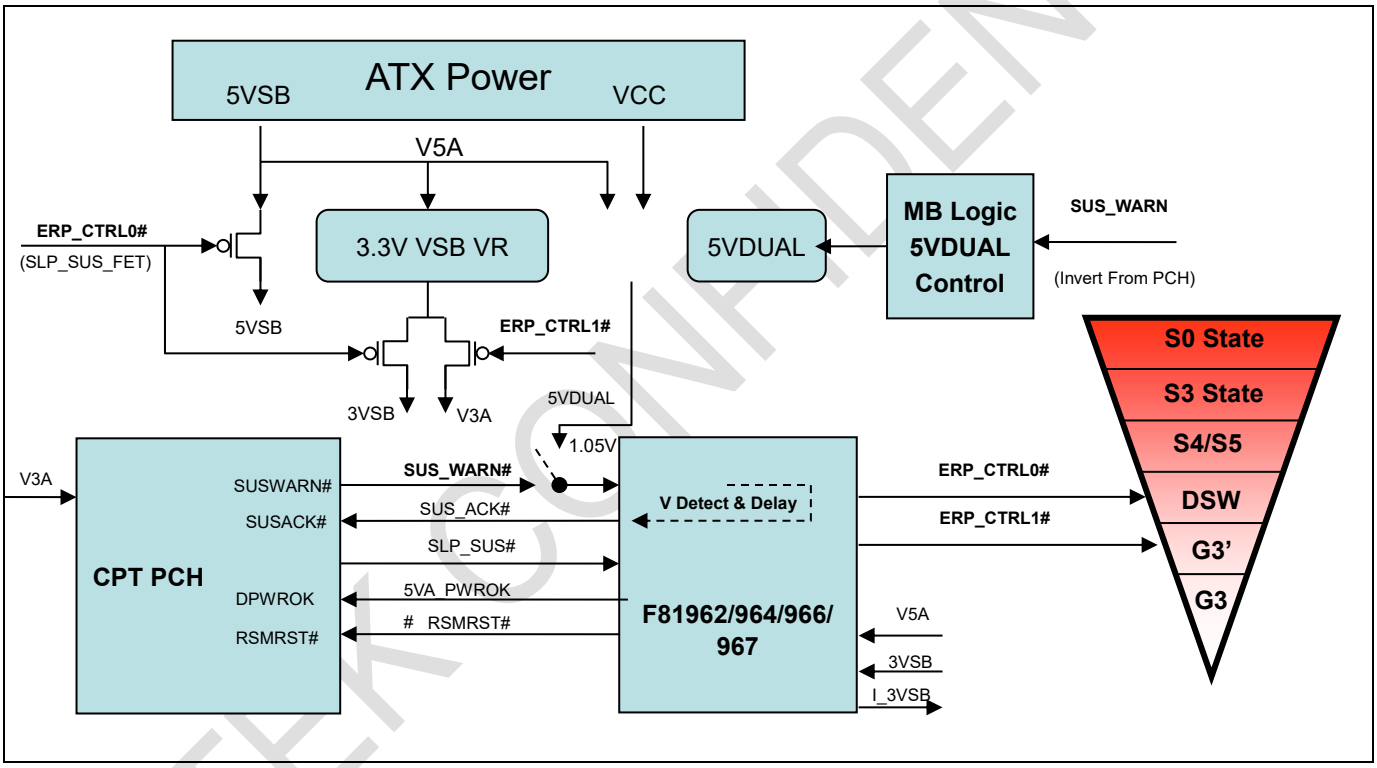
4.6.1.4 Intel Power Saving Function Deep Sleep Well (DSW)

The F81962/F81964/F81966/F81967 support Intel Cougar Point (CPT) Chipset timing for Sandy Bridge (Sugar Bay or Huron River Platform). There are 4 pins for CPT control: SUS_WARN#, SUS_ACK#, SLP_SUS# and DPWROK.

For entering the Intel Deep Sleep Well (DSW) state, the PCH will assert SUS_WARN# (low level) and turn off 5VDUAL. After the level of 5VDUAL is lower than 1.05V, F81962/F81964/F81966/F81967 will assert SUS_ACK# to inform PCH it is ready for entering DSW. Finally, PCH will ramp down the internal VccSUS and assert SLP_SUS# to F81962/F81964/F81966/F81967. F81962/F81964/F81966/F81967 will turn off the 5VSB and 3VSB by ERP_CTRL0# and enter the DSW state.

To exit DSW state, PCH will de-assert SLP_SUS#, turn on the SUS rail FETs and ramp up internal 1.05V VccSUS. After the SUS rails voltages are up, RSMRST# will be desserted and the PCH will release SUS_WARN# so that the 5VDUAL will ramp up.

Because the DSW function is controlled by the F81962/F81964/F81966/F81967 instead of controlled by the PCH directly, there will be more wakeup events such as LAN, KB/Mouse, GPIO0x, GPIO1x, SIO RI# wake up rather than the 3 wakeup events (RTC, Power Button and GPIO27) for Intel DSW.



In order to achieve the lower power consumption, F81962/F81964/F81966/F81967 provides the ERP_CTRL1# to turn off the V3A, that the system can enter the Fintek G3' state.

The block diagram below shows how the connection and control method for F81962/F81964/F81966/F81967 and PCH.

The register for setting this mode is at CR0A, index 0xEC [7:6]. When choose Intel DSW mode, ERP_CTRL0#, & ERP_CTRL1# would follow SLP_SUS#. When choose Intel DSW + Fintek G3' mode, ERP_CTRL0# would follows SLP_SUS#, & ERP_CTRL1# will enter Fintek ERP mode after entering DSW mode for 6.4s (default, the time is programmable).

In sum, there are three blocks in this mode (Please refer to the application circuit for the HW schematic):

a. DSW Control Block:

a-1 SLP_SUS#: SIO input pin from CPT PCH SLP_SUS#.

a-2 SUS_WARN#: SIO input pin from CPT PCH SUS_WARN#.

a-3 SUS_ACK#: SIO output pin to CPT PCH SUSACK#.

a-4 DPWROK: SIO output pin to CPT PCH DPWROK.

b. ERP Control Block:

b-1 ERP_CTRL0#: Support “CPT PCH DSW” control mode which is a low active signal to turn on/off 3VSB/5VSB power source by P MOSFET.

b-2 ERP_CTRL1#: Support “Fintek G3’ ” control mode which is a low active signal to turn on/off 3VA/5VA power source by P MOSFET.

4.6.1.5 Power Saving Controller (Fintek ERP Mode)

The two pins, ERP_CTRL0# and ERP_CTRL1#, which control the standby power rail on/off to fulfill the purpose which decreases the power consumption when the system is in the sleep state or the soft-off state. These two pins connected to the external PMOSs and the defaults are high in the sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, the two pins can be programmable to set which power rail to turn on. The programmable register is powered by the battery. So, the setting is kept even the AC power is lost when the register is set. At the power saving state (FINTEK calls it G3’ state), the F81962/F81964/F81966/F81967 consumes 5VSB power rail only to realize a low power consumption system.

The register for setting this mode is at CR0A, index 0xEC [7:6]. When choose Fintek G3’ mode, ERP_CTRL0# & ERP_CTRL1# will enter S5. After entering S5 for 6.4s (default, the time is programmable), these two pins would send high level signal and then cut off all the power sources except ATX_5VSB (power consumption is about 15mW). In order to avoid the inrush current from ATX_5VSB, F81962/F81964/F81966/F81967 also provide the soft start circuits at these two pins. See the related register for the soft start circuit (CR0A, index 0xEC [4]).

In sum, there are two blocks in this mode (Please refer to the application circuit for the HW schematic):

a. EUP Control Block:

ERP_CTRL0# and ERP_CTRL1# are low active signals to turn on/off 5VSB power source by P MOSFET.

b. Wake Up Event Block via:

Power Button	External LAN	PCH Internal LAN	PS2 KB/Mouse	SIO RI#	RTC	GPIO0x/1x
V	V	X	V	V	X	V

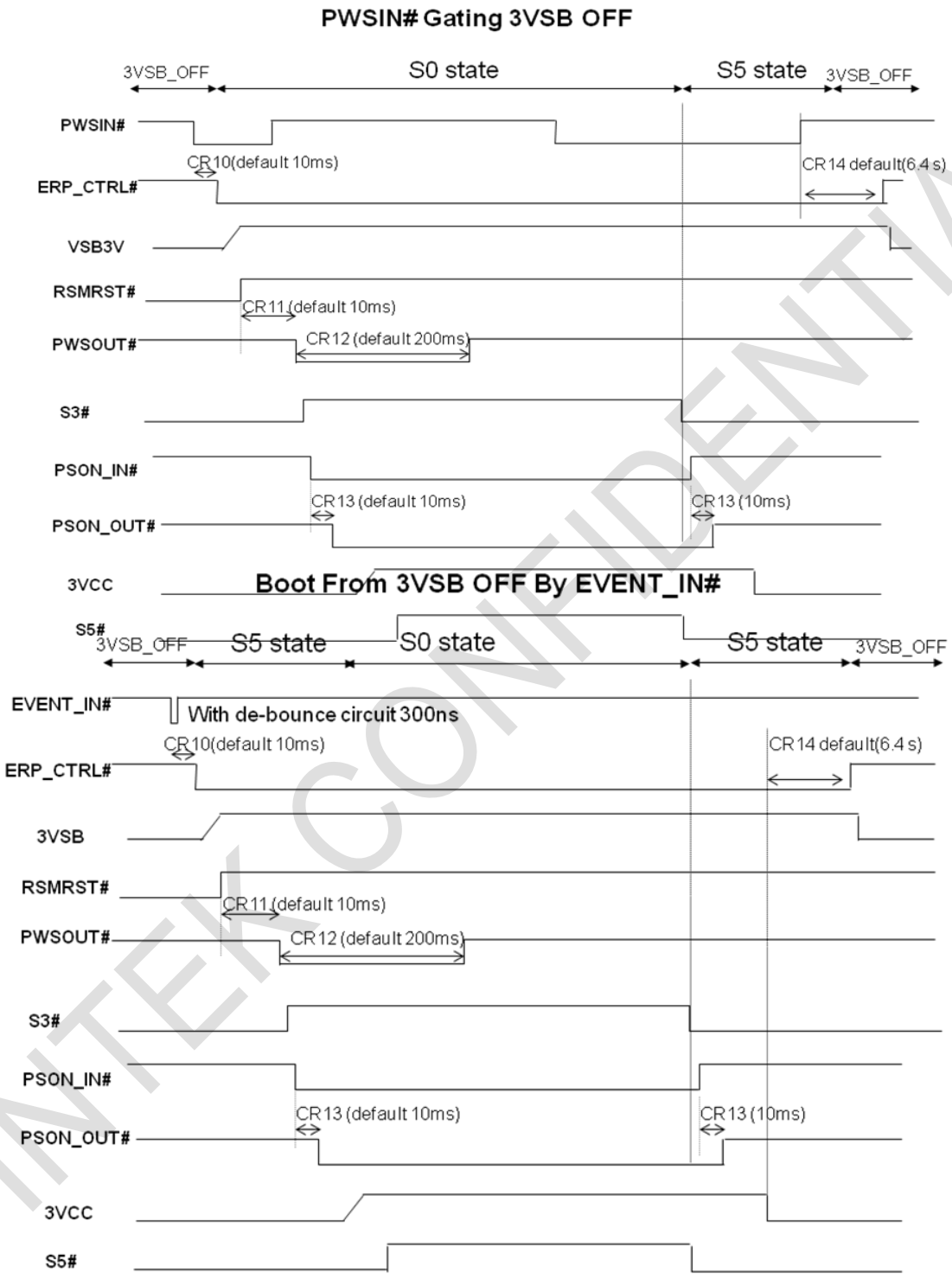
Note:

By pressing/triggering any of the above pin, the system could wake up from the sleep (S4/S5) DSW and G3’ mode.

V: Supported.

X: Does not supported.

4.6.1.6 Fintek G3' (ERP) Timing

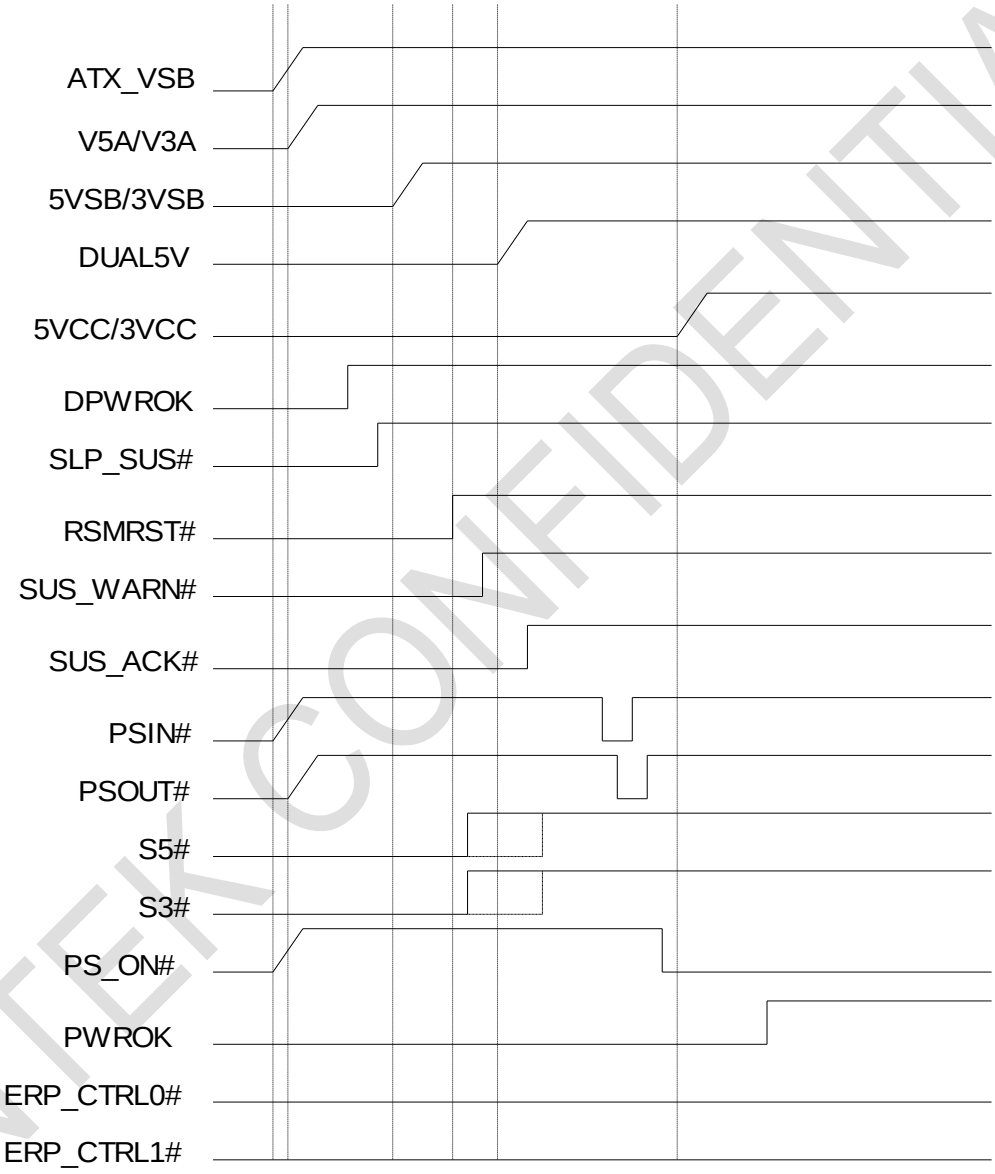


* EVENT_IN# means wake up via GPIO 0x, GPIO 1x, RI#...

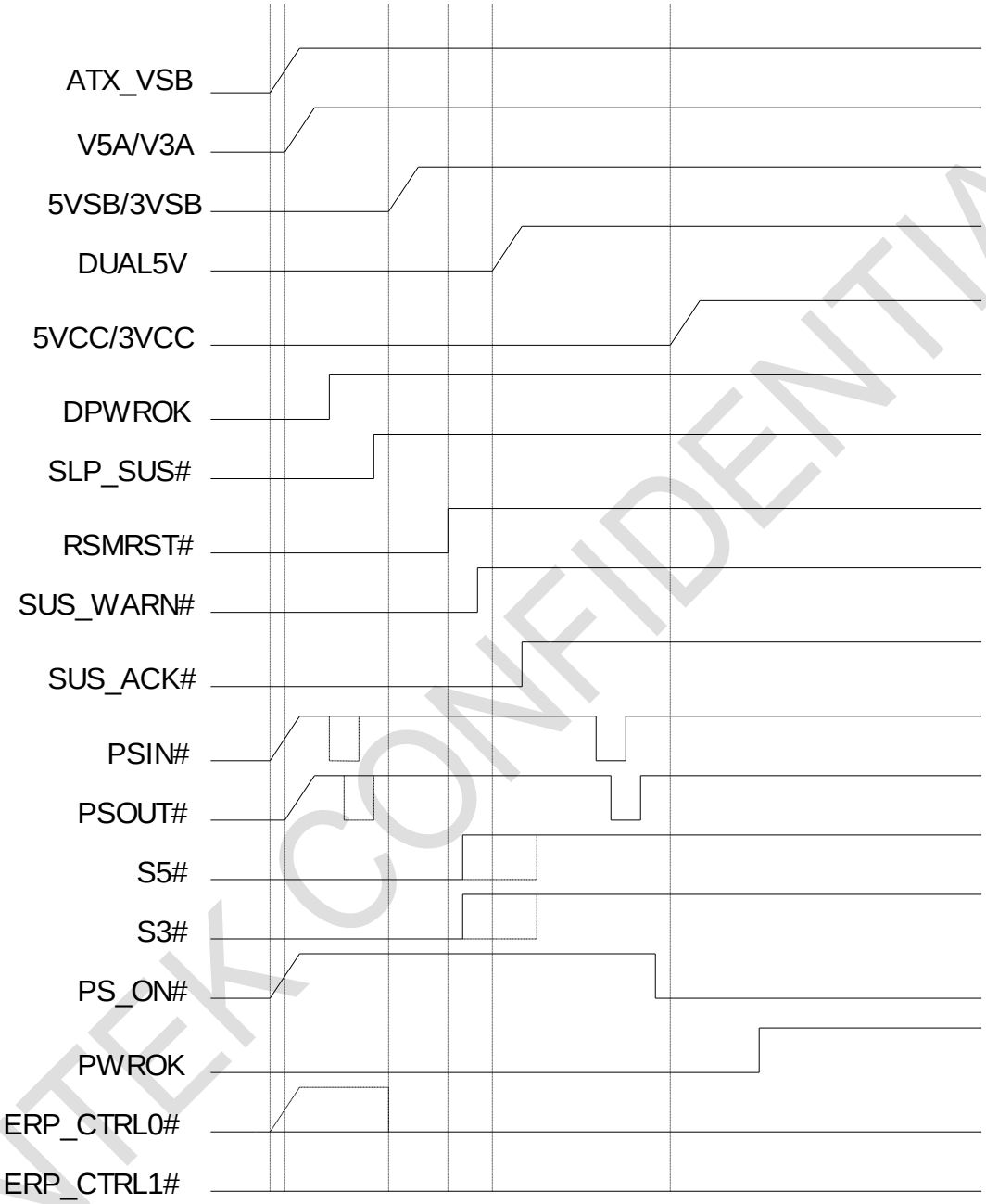
4.6.2 ACPI Timing

See below for the related ACPI timing:

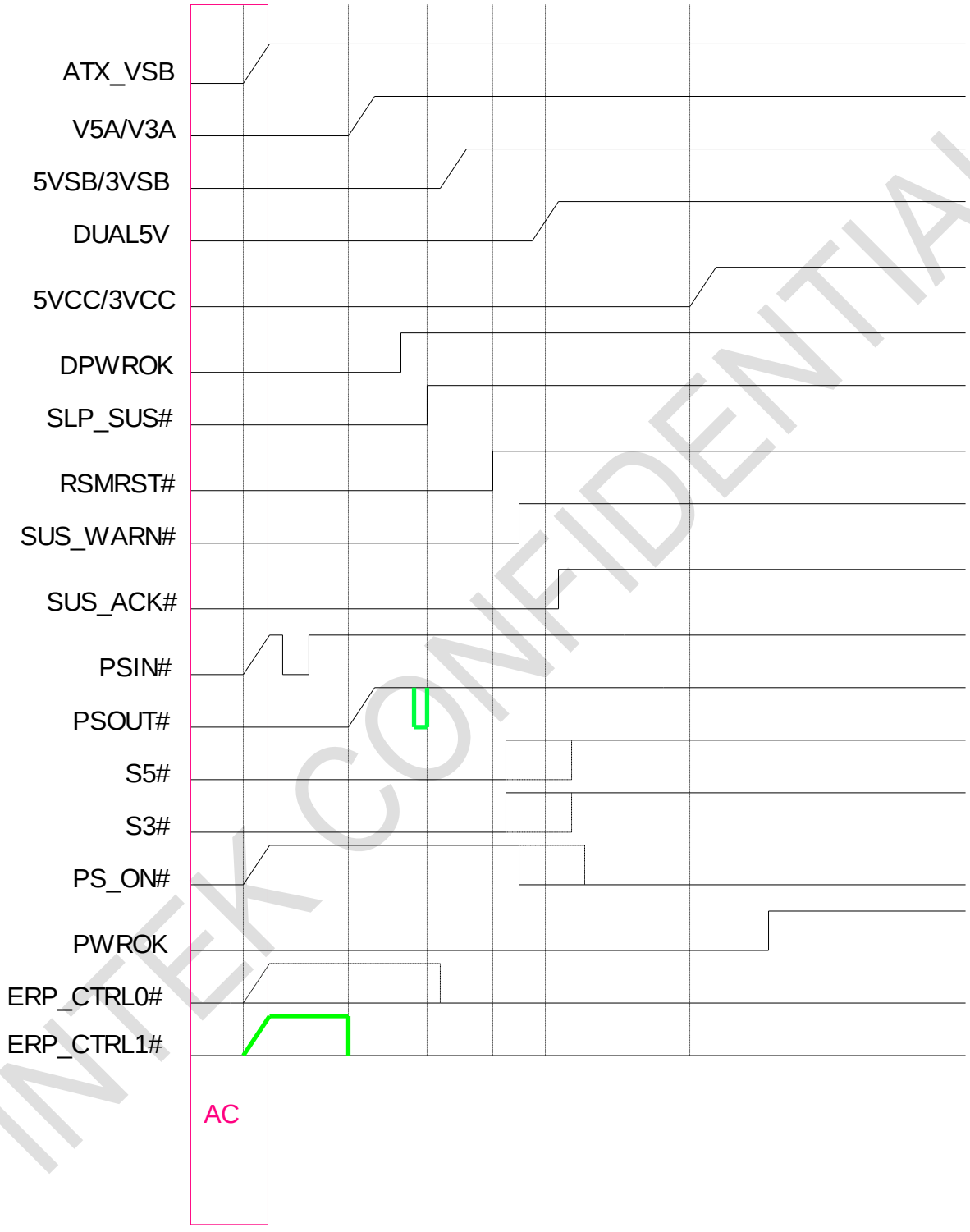
4.6.2.1 G3 To S0



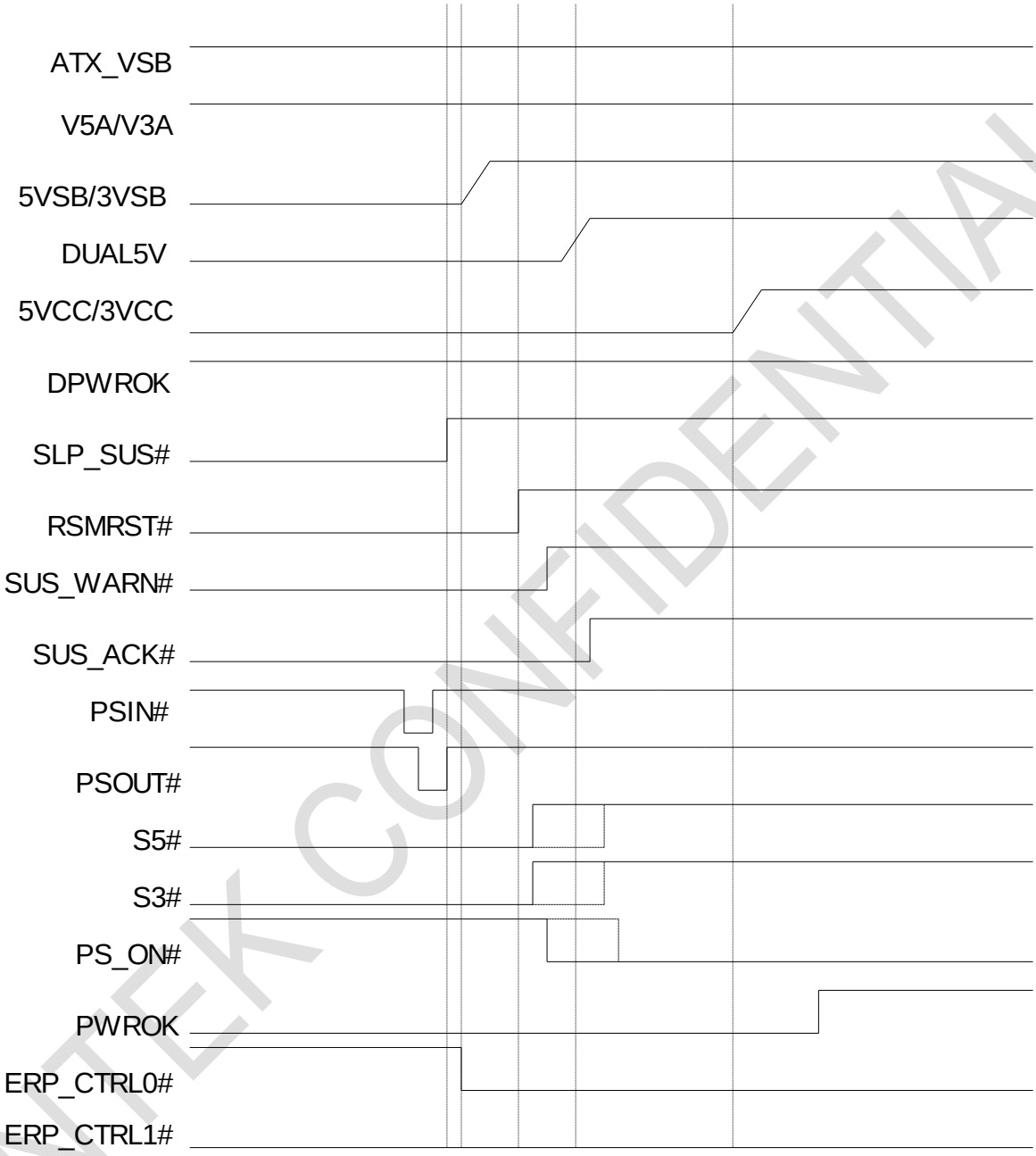
4.6.2.2 G3 To S0 (only DSW)



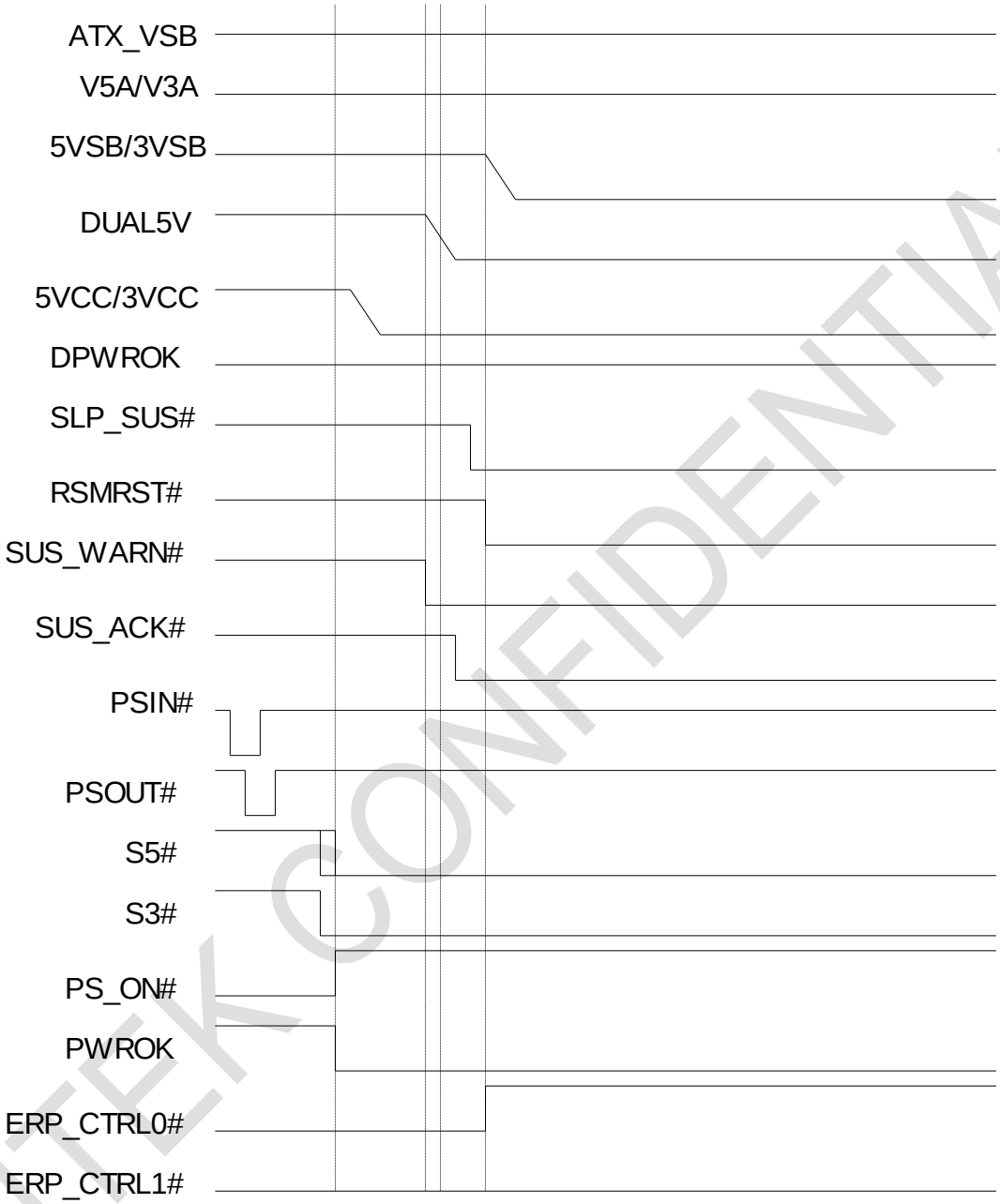
4.6.2.3 G3 To S0 (DSW & ERP, AC Resume Green Bold Line)



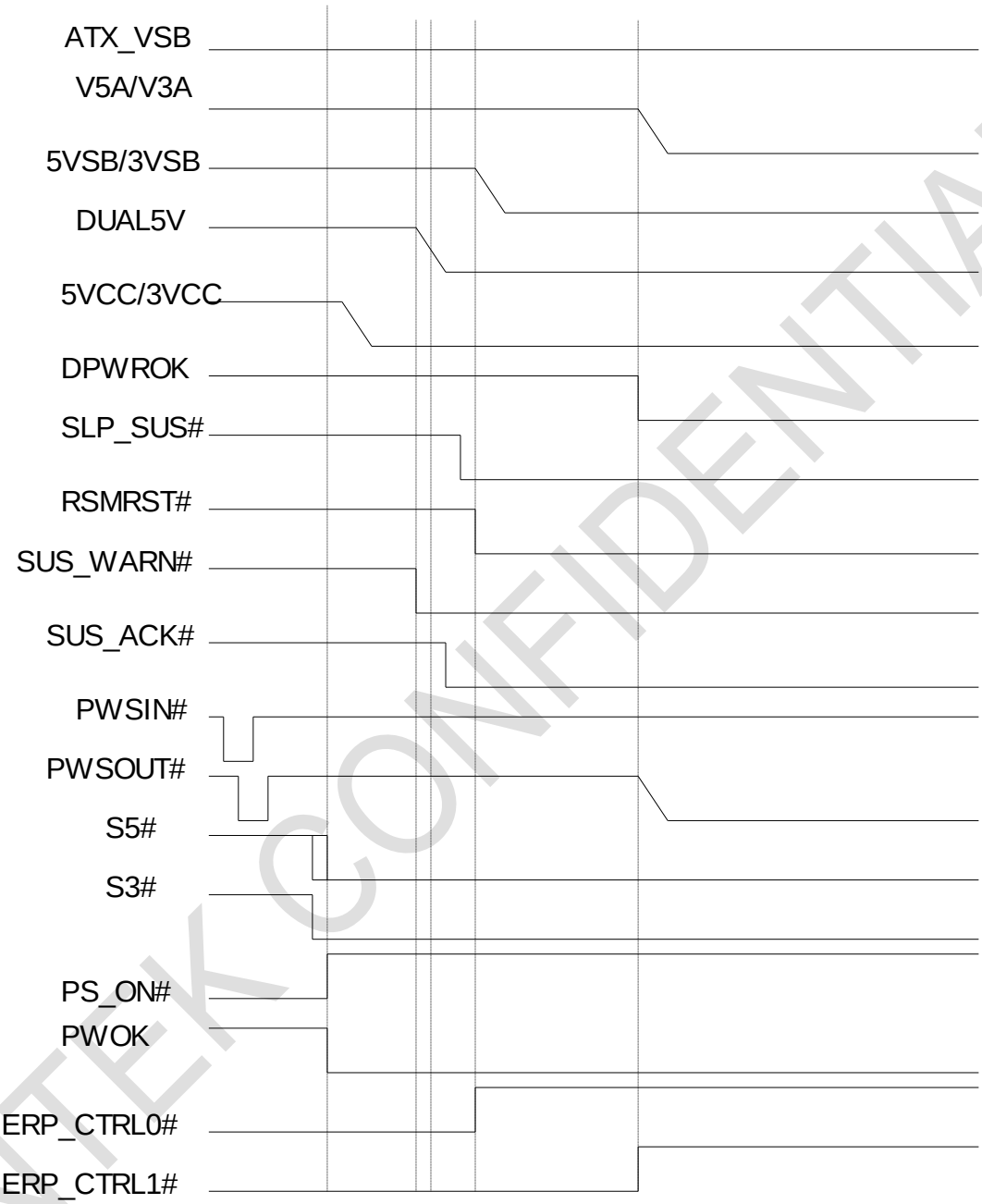
4.6.2.4 **DSW To S0**



4.6.2.5 **S0 to DSW**



4.6.2.6 **S0 to G3'**



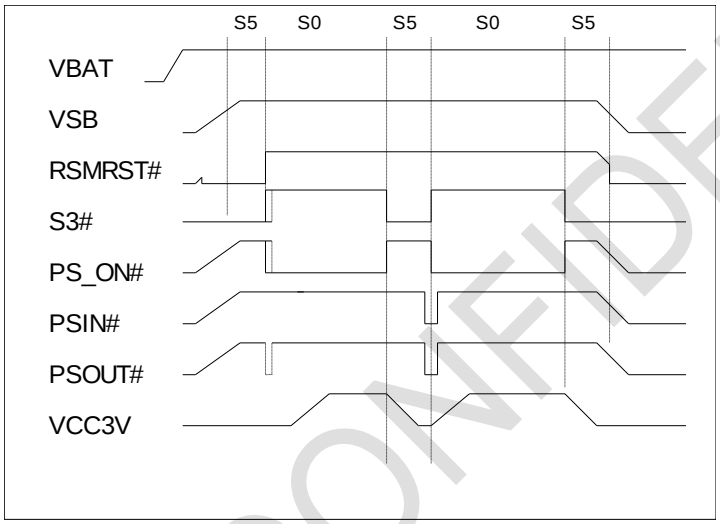
- RSMRST# signal: Powered by VBAT sink low.
- DPWROK/PWROK signal: Powered by VBAT sink low.
- 3VSB 2.8V/2.5V and gate SLP_SUS#/DPWROK for Intel mode

4.6.3 AC Loss & Resume Control Methods

There are 4 modes under power loss state via setting ACPI control register. The always on, always off, keep last state & bypass mode. In keep last state mode, one register will latch the status before power loss. If it is power on before power loss, it will automatically power on when power is resumed. If it is power off before power loss, it will remain power off when power is resumed. See below for the detail:

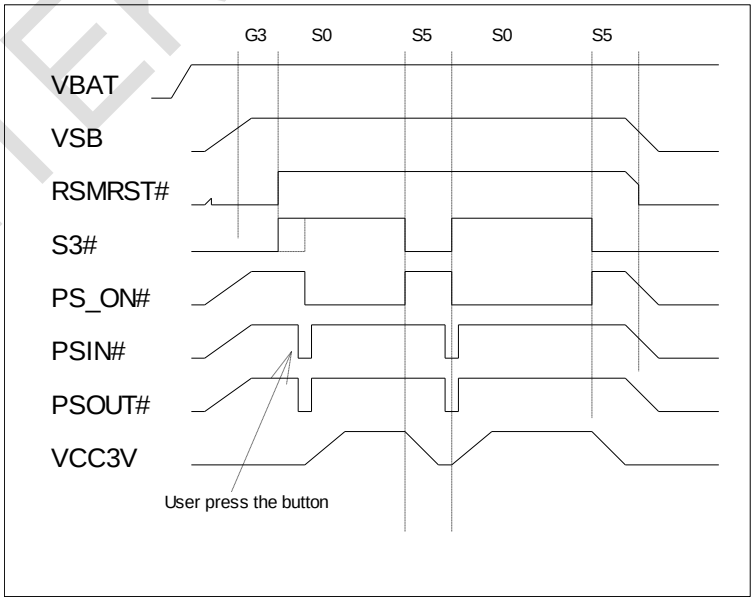
4.6.3.1 **Always on (S0)**

When AC resume, the system will power on automatically (send a PWSOUT# low pulse and then sinking the PS_ON# low). See below for the timing:



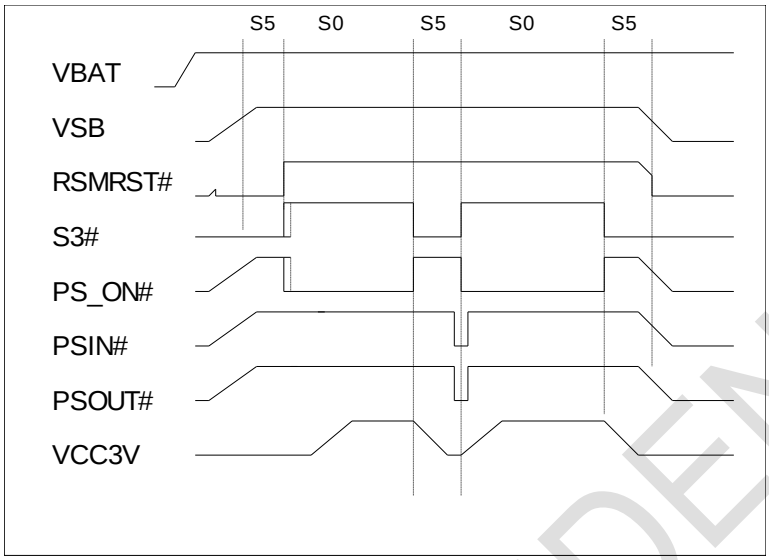
4.6.3.2 **Always off (S5)**

When AC resume, the system is in off state and waiting for the wakeup events. See below for the timing:



4.6.3.3 Bypass (follow the chipset after G3 stage)

When AC resume, inverting the S3 signal to PS_ON#. See below for the timing:



4.6.3.4 Keep last state

ATXPG_IN, VCC (PWROK), VSB (RSMRST) and S3 signals to detect the sleep state while AC loss occur. One of the signal (ATXPG_IN or VCC under 2.8V or VSB under 2.8V) sinks low, SIO will latch the S3 signal to decide the system to be at “always on” or “always off” mode. See below table:

Signal / AC loss state	ATXPG	VSB	VCC	AC resume
AC loss in S0/S1 (S3=1)				Always on
AC loss in S3/S4/S5 (S3=0)				Always off

4.7 UART

The F81962/F81964/F81966/F81967 provide up to 6 UART ports and support IRQ sharing for system application. They are compatible with 16C550/16C650/16C750 and 16C850 .The UARTs are used to convert data between parallel format and serial format. They convert parallel data into serial format on transmission and serial format into parallel data on receiver side. The serial format is formed by one start bit, followed by five to eight data bits, a parity bit if programmed and one (1.5 or 2) stop bits. The UARTs include complete modem control capability and an interrupt system that may be software trailed to the computing time required to handle the communication link. They have FIFO mode to reduce the number of interrupts presented to the host. Both receiver and transmitter have a 128-byte FIFO. The UART control register control & define the asynchronous protocol data communications including data length, stop bit, parity & baud rate selection. The below content is about the UARTs device register descriptions. All the registers are for software porting reference.

4.7.1 UART Device Register

4.7.1.1 Receiver Buffer Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	RBR	R	LRESET#	00h	The data received. Read only when LCR [7] is 0

4.7.1.2 Transmitter Holding Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	THR	W	LRESET#	00h	Data to be transmitted. Write only when LCR [7] is 0

4.7.1.3 Divisor Latch (LSB) — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	DLL	R/W	LRESET#	01h	Baud generator divisor low byte. Access only when LCR [7] is 1.

4.7.1.4 Divisor Latch (MSB) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-0	DLM	R/W	LRESET#	00h	Baud generator divisor high byte. Access only when LCR [7] is 1.

4.7.1.5 Interrupt Enable Register (IER) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.

4	SM2	R/WC	LRESET#	0	This bit is used only in 9-bit mode and always returns “0” when 9-bit mode is disabled. 0: The receiver could receive data byte. 1: The receiver could only receive address byte and issue an interrupt when the address is received.
3	EDSSI	R/W	LRESET#	0	Enable Modem Status Interrupt. Access only when LCR [7] is 0.
2	ELSI	R/W	LRESET#	0	Enable Line Status Error Interrupt. Access only when LCR [7] is 0.
1	ETBFI	R/W	LRESET#	0	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR [7] is 0.
0	ERBFI	R/W	LRESET#	0	Enable Received Data Available Interrupt. Access only when LCR [7] is 0.

4.7.1.6 Interrupt Identification Register (IIR) — Base + 2

Bit	Name	R/W	Reset	Default	Description
7	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
6	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
5-4	Reserved	-	LRESET#	-	Reserved.
3-1	IRQ_ID	R	LRESET#	00	000: Interrupt is caused by Modem Status 001: Interrupt is caused by Transmitter Holding Register Empty 010: Interrupt is caused by Received Data Available. 110: Interrupt is caused by Character Timeout 011: Interrupt is caused by Line Status.
0	IRQ_PENDN	R	LRESET#	1	1: Interrupt is not pending. 0: Interrupt is pending.

4.7.1.7 FIFO Control Register — Base + 2

Bit	Name	R/W	Reset	Default	Description
7-6	RCV_TRIG	W	LRESET#	00	00: Receiver FIFO trigger level is 1. 01: Receiver FIFO trigger level is 4. 10: Receiver FIFO trigger level is 8. 11: Receiver FIFO trigger level is 14.
5-3	Reserved	-	LRESET#	-	Reserved.
2	CLRTX	R	LRESET#	0	Reset the transmitter FIFO.
1	CLRRX	R	LRESET#	0	Reset the receiver FIFO.
0	FIFO_EN	R	LRESET#	0	0: Disable FIFO. 1: Enable FIFO.

4.7.1.8 Line Control Register (LCR) — Base + 3

Bit	Name	R/W	Reset	Default	Description
7	DLAB	R/W	LRESET#	0	0: Divisor Latch can't be accessed. 1: Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	LRESET#	0	0: Transmitter is in normal condition. 1: Transmit a break condition.
5	STKPAR	R/W	LRESET#	0	XX0: Parity Bit is disable 001: Parity Bit is odd. 011: Parity Bit is even 101: Parity Bit is logic 1 111: Parity Bit is logic 0
4	EPS	R/W	LRESET#	0	
3	PEN	R/W	LRESET#	0	
2	STB	R/W	LRESET#	0	0: Stop bit is one bit 1: When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1-0	WLS	R/W	LRESET#	00	00: Word length is 5 bit 01: Word length is 6 bit 10: Word length is 7 bit 11: Word length is 8 bit

4.7.1.9 MODEM Control Register (MCR) — Base + 4

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	LRESET#	-	Reserved.
4	LOOP	R/W	LRESET#	0	0: UART in normal condition. 1: UART is internal loop back
3	OUT2	R/W	LRESET#	0	0: All interrupt is disabled. 1: Interrupt is enabled (disabled) by IER.
2	OUT1	R/W	LRESET#	0	Read from MSR[6] while in loop back mode
1	RTS	R/W	LRESET#	0	0: RTS# is forced to logic 1 1: RTS# is forced to logic 0
0	DTR	R/W	LRESET#	0	0: DTR# is forced to logic 1 1: DTR# is forced to logic 0

4.7.1.10 Line Status Register (LSR) — Base + 5

Bit	Name	R/W	Reset	Default	Description
7	RCR_ERR	R	LRESET#	0	0: No error in the FIFO when FIFO is enabled 1: Error in the FIFO when FIFO is enabled.
6	TEMT	R	LRESET#	1	0: Transmitter is in transmitting. 1: Transmitter is empty.
5	THRE	R	LRESET#	1	0: Transmitter Holding Register is not empty. 1: Transmitter Holding Register is empty.

4	BI	R	LRESET#	0	0: No break condition detected. 1: A break condition is detected.
3	FE	R	LRESET#	0	0: Data received has no frame error. 1: Data received has frame error.
2	PE	R	LRESET#	0	0: Data received has no parity error. 1: Data received has parity error.
1	OE	R	LRESET#	0	0: No overrun condition occurred. 1: An overrun condition occurred.
0	DR	R	LRESET#	0	0: No data is ready for read. 1: Data is received.

4.7.1.11 MODEM Status Register (MSR) — Base + 6

Bit	Name	R/W	Reset	Default	Description
7	DCD	R	-	-	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	-	-	Complement of RI# input. In loop back mode , this bit is equivalent to OUT1 in MCR
5	DSR	R	-	-	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	-	-	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	LRESET#	0	0: No state changed at DCD#. 1: State changed at DCD#.
2	TERI	R	LRESET#	0	0: No Trailing edge at RI#. 1: A low to high transition at RI#.
1	DDSR	R	LRESET#	1	0: No state changed at DSR#. 1: State changed at DSR#.
0	DCTS	R	LRESET#	1	0: No state changed at CTS#. 1: State changed at CTS#.

4.7.1.12 Scratch Register — Base + 7

Bit	Name	R/W	Reset	Default	Description
7-0	SCR	R/W	LRESET#	00h	Scratch register.

4.7.2 Programmable Baud Rate

The below table shows the use of baud generator with the different frequency 1.8461 MHZ, 18.461 MHZ, 14.769 MHZ, 24MHZ:

$$\text{BaudRate} = \frac{\text{COM\_CLK}}{\text{Divisor} * 16}$$

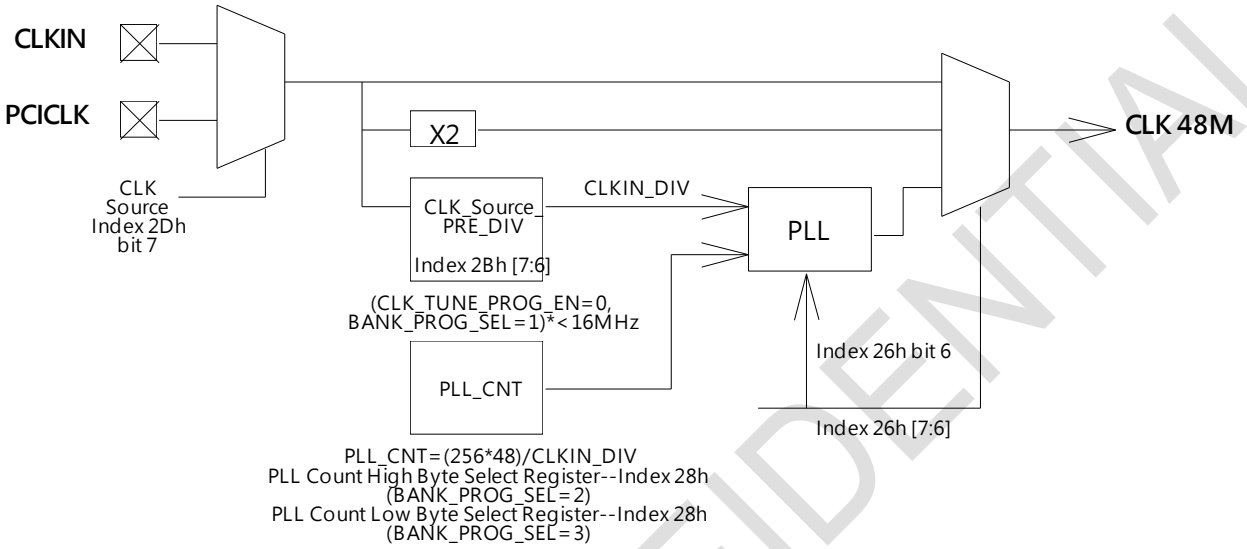
BAUD RATE FROM DIFFERENT PRE-DIVIDER					
PRE-DIV: 13 1.8461 MHz	**PRE-DIV: 1.625 14.769 MHz**	**PRE-DIV: 1.3 18.461 MHz**	**PRE-DIV: 1.0 24 MHz**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERECNTAGE**
50	400	500	650	2308	0
75	600	7500	975	1538	0
110	880	1100	1430	1049	0
135	1080	1350	1755	855	0
150	1200	1500	1950	769	0
300	2400	3000	3900	385	0
600	4800	6000	7800	192	0
1200	9600	12000	15600	96	0
1800	14400	18000	23400	64	0.01%
2000	16000	20000	26000	58	0.01%
2400	19200	24000	31200	48	0.01%
3600	28800	36000	46800	32	0.01%
4800	38400	48000	62400	24	0.01%
7200	57600	72000	93600	16	0.01%
9600	76800	96000	124800	12	0.01%
19200	153600	192000	249600	6	0.01%
38400	307200	384000	499200	3	0.01%
57600	460800	576000	748800	2	0.01%
115200	921600	1152000	1497600	1	0.01%

Example 1 : $1.5\,\text{MHz} = \frac{24}{1*16}$ **Example 2 :** $0.576\,\text{MHz} = \frac{18.461}{2*16}$

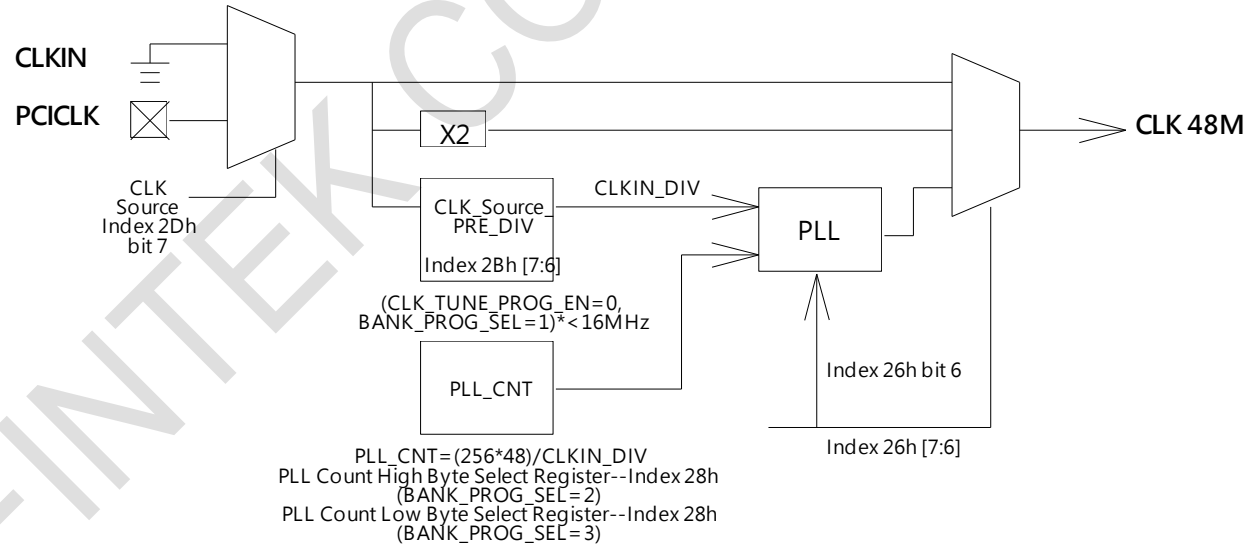
4.8 CLKIN

The clock in is programmable with the internal register. Please check below figure for the detail flow:

Option A. CLKIN input 24M/48MHz or 10M~50M Hz input ; PCI clock 10M~33 MHz input.



Option B. Without CLKIN for system clock, the system clock is programmable by the internal register(only for LPC).
PCI clock 10M~33 MHz input.



5 Configuration Register

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the RTS1# pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following an example to enable configuration and disable configuration by using debug.

-o 4E 87
-o 4E 87 (enable configuration)
-o 4E AA (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer to each device chapter if you want more detail information.

5.1 Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value** MSB LSB							
02	Software Reset Register	-	-	-	-	-	-	-	-
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	1	0	1	0	1
21	Chip ID Register	0	0	0	0	0	0	1	0
23	Vendor ID Register	0	0	0	1	1	0	0	1
24	Vendor ID Register	0	0	1	1	0	1	0	0
25	I2C Address Register	-	-	-	-	-	-	-	0
26	Clock Select Register	0	0	1	0	0	0	1	1
27	Port Select Register	1/0	1/0	0	1/0	0	0	1	0
28	Multi Function Select Register 1 (BANK_PROG_SEL = 0)	1	0	1	0	0	0	0	0
28	Multi Function Select Register 2 (BANK _PROG_SEL = 1)	0	0	0	0	0	0	0	0
28	CLKIN Count High Byte Select Register (BANK _PROG_SEL = 2)	0	0	0	0	0	0	1	1
28	CLKIN Count Low Byte Select Register (BANK _PROG_SEL = 3)	0	1	0	1	1	0	1	1
29	Multi Function Select Register 3 (CLK_TUNE_PROG_EN = 0)	0	0	0	0	0	0	0	0
29	ERP Clock Fine Tune High Byte Register (CLK_TUNE_PROG_EN = 1)	-	-	-	-	0	0	1	1
2A	GPIO1 Function Select Register 1 (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 0)	0	0	0	0	0	0	0	0
2A	GPIO1 Function Select Register 2 (CLK_TUNE_PROG_EN = 0; BANK _PROG_SEL = 1)	0	0	0	0	0	0	0	0
2A	GPIO1 Function Select Register 3 (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 2)	0	1	1	0	0	0	0	0

2A	GPIO1 Function Select Register 4 (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 3)	0	0	0	0	0	0	1	1
2A	ERP Clock Fine Tune Low Byte Register (CLK_TUNE_PROG_EN = 1)	1	1	1	0	0	1	1	1
2B	Multi Function Select Register 4 (CLK_TUNE_PROG_EN = 0)	0	0	0	0	0	0	1	0
2B	Clock Control Register (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 1)	0	0	0	0	0	0	0	0
2B	TSI/MXM Pin Select Register (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 2)	0	0	0	0	0	0	0	0
2B	I2C Pin Select Register (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 3)	0	0	0	0	0	0	0	0
2B	ERP Clock Count High Byte With A Period Register (CLK_TUNE_PROG_EN = 1)	-	-	-	-	-	-	-	-
2C	Multi Function Select Register 5 (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 0)	-	-	-	0	1	1	0	0
2C	Enable I2C Pin Register (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 1)	0	0	0	0	0	0	0	0
2C	Multi Function Select Register 6 (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 2)	0	0	0	0	0	0	0	0
2C	Multi Function Select Register 7 (CLK_TUNE_PROG_EN = 0; BANK_PROG_SEL = 3)	0	0	0	1	1	0	0	0
2C	ERP Clock Fine Tune Low Byte With A Period Register (CLK_TUNE_PROG_EN = 1)	0	0	0	0	0	0	0	0
2D	Wakeup Control Register	0	0	1	0	1	0	0	0

5.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	SOFT_RST	W	-	-	Write 1 to reset the register and device powered by VDD (VCC).

5.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LREST#	00h	03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. 0Eh: Select E2L device configuration registers. 0Fh: Select SPI device configuration registers. 10h: Select UART1 device configuration registers. 11h: Select UART2 device configuration registers. 12h: Select UART3 device configuration registers. 13h: Select UART4 device configuration registers. 14h: Select UART5 device configuration registers. 15h: Select UART6 device configuration registers. Otherwise: Reserved.

5.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIP_ID1	R	-	15h	Chip ID 1.

5.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Reset	Default	Description
7-0	CHIP_ID2	R	-	02h	Chip ID2.

5.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID1	R	-	19h	Vendor ID 1.

5.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Reset	Default	Description
7-0	VENDOR_ID2	R	-	34h	Vendor ID 2.

5.1.7 I2C Address Select Register — Index 25h

Bit	Name	R/W	Reset	Default	Description
7-1	I2C_ADDR	R/W	5VSB	-	I2C Slave Address. This byte is power-on strap by SOUT1 pin. 1: 7'h2E 0: 7'h2D If this byte is programmed, the value will keep and power-on strap has no effect until 5VSB lost.
0	EN_ARA_MODE	R/W	5VSB	0	0: Disable ARA mode. 1: Enable ARA mode.

5.1.8 Clock Select Register — Index 26h

Bit	Name	R/W	Reset	Default	Description
7-6	CLK_SEL	R/W	5VSB	00	The clock source of CLKIN. 00: CLKIN is 48MHz 10: CLKIN is 24MHz X1: CLKIN is programmable(only for LPC).
5-4	ENTRY_KEY_SEL	R/W	5VSB	10	Select the entry key for configuration registers. (Only for F81967) 00: 0x77. 01: 0xA0. 10: 0x87. 11: 0x67.
3	PIN76_LVL_SEL	R/W	5VSB	0	PIN 76 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
2	PIN71_LVL_SEL	R/W	5VSB	0	PIN 71 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
1	PIN68_LVL_SEL	R/W	5VSB	1	PIN 68 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.
0	PIN67_LVL_SEL	R/W	5VSB	1	PIN 67 input level select. 0: TTL level. 1: Low level with 0.6V low and 0.9V high.

5.1.9 Port Select Register — Index 27h

Bit	Name	R/W	Reset	Default	Description
7	OVP_MODE	R/W	VBAT	1	OVP/UVP mode select. 0: OVP/UVP is auto enabled after power on. 1: OVP/UVP is enabled by registers. This bit is power-on strap by DTR2#.

6	AT_MODE	R/W	VBAT	0	0: ATX Mode. 1: AT Mode. The default value is determined by power on strap when power on.
5	GPIO_DEC_RANGE	R/W	3VCC	0	0: The GPIO I/O space is 8-byte. 1: The GPIO I/O space is 16-byte.
4	PORT_4E_EN	R/W	3VCC	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by RTS1#/ STRAP4E_2E. Pull down to select port 2E/2F.
3-2	BANK_PROG_SEL	R/W	5VSB	0	Bank select for configuration registers (bank 0/1/2/3). BANK0 → 0x27[3:2] = 00; 0x27[0] = 0 BANK1 → 0x27[3:2] = 01; 0x27[0] = 0 BANK2 → 0x27[3:2] = 10; 0x27[0] = 0 BANK3 → 0x27[3:2] = 11; 0x27[0] = 0
1	DPORT_EN	R/W	3VCC	1	0: Disable 0x80 port. 1: Enable 0x80 port. This register is power on trapped by SOUT2.
0	CLK_ TUNE_PROG_EN	R/W	3VCC	0	Set “1” to enable ErP clock fine tune registers.

5.1.10 Multi-function Select Register 1 — Index 28h (Available when BANK_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7	PECI_PIN_EN	R/W	VBAT	1	PECI/GPIO17 pin function select. 0: GPIO17. 1: PECI.
6	LPT_PD_EN	R/W	VBAT	0	Set “1” to enable parallel port (LPT: printer) PD pins. It has no effect if LPC_M_EN is set or DPORT_EN pin is selected as PD pins.
5	LPT_GP_EN	R/W	VBAT	1	GPIO7x/GPIO8x and parallel port (LPT: printer) pins function select. 0: LPT pins. 1: GPIO7x and GPIO8x.
4	IR_PIN_EN	R/W	VBAT	0	GPIO12/IRTX and GPIO13/IRRX pin function select. 0: GPIO12 and GPIO13. 1: IRTX and IRRX.
3-2	UR5_GP_EN	R/W	VBAT	0	UART5 pin function select. 00: All pins are function as GPIO. 01: Simple UART, only SIN5 and SOUT5 are available. Pin 57 will be function as SOUT5 and Pin 58 will be function as SIN5. Pin 17 ~21 and Pin 59 are GPIOs. 10: Simple UART, use pin 58 as SIN5, pin 57 as SOUT5 and Pin 59 as RTS5# function. Pin 17 ~ 21 are as GPIOs. 11: Full UART. Pin 57 ~ 59, 17 ~ 21 will function as UART 5 pins. * UART 5 function is only active for F81966

1-0	UR6_GP_EN	R/W	VBAT	0	UART6 pin function select. 00: All pins are function as GPIO. 01: Simple UART, only SIN6 and SOUT6 are available. Pin 11 will be function as SOUT6 and Pin 10 will be function as SIN6. Pin 9 and Pin 12 ~16 are GPIOs. 10: Simple UART, use pin 10 as SIN6, pin 11 as SOUT6 and Pin 9 as RTS6# function. Pin 12 ~ 16 are as GPIOs. 11: Full UART, pin 9 ~ 16 will function as UART 6 pins. *UART 6 function is only active for F81966

5.1.11 Multi-function Select Register 2 — Index 28h (Available when BANK_PROG_SEL= 1)

Bit	Name	R/W	Reset	Default	Description
7	ERR_VWIRE_EN	R/W	VBAT	0	0 : Disable eSPI fetal error and nonfetal error. 1 : Enable eSPI fetal error and nonfetal error.
6	DPORT_PIN_SEL	R/W	VBAT	0	Select pins for 0x80 port. 0: Pin 111-118. 1: Pin 9-16.
5	SPI_PIN_SEL	R/W	VBAT	0	Select pins for SPI master when SPI_PIN_EN is set. 0: Pin 107-110. 1: Pin 13-16.
4	SPI_PIN_EN	R/W	VBAT	0	Set “1” to enable SPI master pins.
3	DPORT_MODE	R/W	VBAT	0	0: Debug port output 0x80 port value which is converted into 7-segment LED. 1: Debug port output 0x80 port value directly.
2	SIRQ_PWR_SEL	R/W	VBAT	0	0: SIRQ pin is powered by IFP(pin 31). 1: SIRQ pin is powered by internal 1.8V. (only used when IFP is 3.3V) This bit doesn’t has effect in eSPI interface.
1	GA20_PU_DIS	R/W	VBAT	0	0: Enable GA20 internal 10K pull-up. 1: Disable GA20 internal 10K pull-up.
0	KBRST_PU_DIS	R/W	VBAT	0	0: Enable KBRST internal 10K pull-up. 1: Disable KBRST internal 10K pull-up.

5.1.12 PLL Count High Byte Select Register — Index 28h (BANK_PROG_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7-0	PLL_CNT_H	R/W	VBAT	3h	PLL_CNT is composed by PLL_CNT_H and PLL_CNT_L which are used to indicate the clock generator to generate 48MHz according the CLKIN_DIV. PLL_CNT is calculated by the equation: PLL_CNT = (256*48) / CLKIN_DIV.

5.1.13 PLL Count Low Byte Select Register — Index 28h (BANK_PROG_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7-0	PLL_CNT_L	R/W	VBAT	5Bh	PLL_CNT is composed by PLL_CNT_H and PLL_CNT_L which are used to indicate the clock generator to generate 48MHz according the CLKIN_DIV. PLL_CNT is calculated by the equation: PLL_CNT = (256*48) / CLKIN_DIV.

5.1.14 Multi Function Select Register 3 — Index 29h (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	UR4_GP_EN	R/W	VBAT	00	UART4 pin function select. 00: All pins function as GPIO. 01: Simple UART, only SIN4 and SOUT4 are available. Pin 50 will be function as SOUT4 and Pin 51 will be function as SIN4. Pin 44 ~ 49 are GPIOs. 10: Simple UART use pin 50 as SOUT4, pin 51 as SIN4, and pin 48 as RTS4# function. Pin 44 ~ 47 and Pin 49 are as GPIOs. 11: Full UART, pin 44 ~ 51 will be all function as UART pins. * UART 4 function is only active for F81966 & F81964
5-4	UR3_GP_EN	R/W	VBAT	00	UART3 pin function select. 00: All pins function as GPIO. 01: Simple UART, only SIN3 and SOUT3 are available. Pin 42 will be function as SOUT3 and Pin 43 will be function as SIN3. Pin 36 ~ 41 are GPIOs. 10: Simple UART use pin 42 as SOUT3, pin 43 as SIN3, and pin 40 as RTS3# function. Pin 36 ~ 39 and Pin 41 are as GPIOs. 11: Full UART, pin 36 ~ 43 will be function as UART pins. * UART 3 function is only active for F81966 & F81964
3	MO_PIN_LVL_SEL	R/W	VBAT	0	Pin 61/62 input level select. 0: TTL level. 1: Low input level.
2	Reserved	R/W	VBAT	0	Dummy registers.
1	P55_LVL_SEL	R/W	VBAT	0	Pin 55 input level select. 0: TTL level. 1: Low input level.
0	P54_LVL_SEL	R/W	VBAT	0	Pin 54 input level select. 0: TTL level. 1: Low input level.

5.1.15 ERP Clock Fine Tune Divisor High Byte Register — Index 29h (CLK_TUNE_PORG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7	CLK_TUNE	W	-	-	Write “1” to start count for clock fine tune.
6-4	Reserved	-	-	-	Reserved.
3-0	CLK_TUNE_DIV [11:8]	R/W	VBAT	3h	ErP 10Hz clock is calculated by Internal 10KHz/CLK10HZ_DIV. User should read CLK_TUNE_CNT to determine the error and program CLK_TUNE_DIV to fine tune the clock.

5.1.16 GPIO1 Function Select Register 1 — Index 2Ah (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	VBAT	0	Dummy register for future use.
6-4	GPIO11_FUNC_SEL	R/W	VBAT	0	GPIO11 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.
3	Reserved	R/W	VBAT	0	Dummy register for future use.
2-0	GPIO10_FUNC_SEL	R/W	VBAT	0	GPIO10 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.

5.1.17 GPIO1 Function Select Register 2 — Index 2Ah (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	VBAT	0	Dummy register for future use.
6-4	GPIO13_FUNC_SEL	R/W	VBAT	0	GPIO13 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.
3	Reserved	R/W	VBAT	0	Dummy register for future use.
2-0	GPIO12_FUNC_SEL	R/W	VBAT	0	GPIO12 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.

5.1.18 GPIO1 Function Select Register 3 — Index 2Ah (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	VBAT	0	Dummy register for future use.
6-4	GPIO15_FUNC_SEL	R/W	VBAT	6h	GPIO15 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.
3	Reserved	R/W	VBAT	0	Dummy register for future use.

2-0	GPIO14_FUNC_SEL	R/W	VBAT	0	GPIO14 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.

5.1.19 GPIO1 Function Select Register 4 — Index 2Ah (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	VBAT	0	Dummy register for future use.
6-4	GPIO17_FUNC_SEL	R/W	VBAT	0	GPIO17 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.
3	Reserved	R/W	VBAT	0	Dummy register for future use.
2-0	GPIO16_FUNC_SEL	R/W	VBAT	3h	GPIO16 function select 000: GPIO. 001: PME#. 010: CLKOUT. 011: BEEP. 100: LED_VCC. 101: LED_VSB. 110: WDTRST#. 111: ALERT#.

5.1.20 ERP Clock Fine Tune Divisor Low Byte Register — Index 2Ah (CLK_TUNE_PORG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	CLK_TUNE_DIV[7:0]	R/W	VBAT	E7h	ErP 10Hz clock is calculated by Internal 10KHz/CLK10HZ_DIV. User should read CLK_TUNE_CNT to determine the error and program CLK_TUNE_DIV to fine tune the clock.

5.1.21 Multi Function Select Register 4 — Index 2Bh (Available when CLK_ TUNE_PROG_EN = 0)

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_EN	R/W	VBAT	0	Pin 87 function select 0: Pin 87 functions as S5#. 1: Pin 87 functions as GPIO67.
6	GPIO66_EN	R/W	VBAT	0	Pin 86 function select 0: Pin 86 functions as DPWROK. 1: Pin 86 functions as GPIO66.
5	GPIO65_EN	R/W	VBAT	0	Pin 74 function select 0: Pin 74 functions as PME#. 1: Pin 74 functions as GPIO65.
4-2	Reserved	R/W	VBAT	0	Dummy register for future use.
1	FANIN3_EN	R/W	VBAT	1	Pin 102 function select 0: Pin 102 functions as SCLT/GPIO97. 1: Pin 102 functions as FANIN3.
0	FANCTL3_EN	R/W	VBAT	0	Pin 103 function select. 0: Pin 103 functions as GPIO70/PE. 1: Pin 103 functions as FANCTL3.

5.1.22 Clock Control Register — Index 2Bh (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-6	CLK_Source_PRE_DIV	R/W	VBAT	0	These registers are used to calculate CLKIN_DIV to generate internal 48MHz clock where the calculated CLKIN_DIV value should be under 16MHz. The equation is as follow: CLKIN_DIV = Clock Source / (CLKIN_PRE_DIV), where CLKIN_PRE_DIV value is 00: bypass 01:divided by 2 10:divided by 4 11:divided by 6
5-4	CLKOUT_PRE_DIV	R/W	VBAT	0	CLKOUT Divisor CLKOUT = 48MHz / (CLKOUT_PRE_DIV * 2) ; 0 means 48MHz.
3	LPC_M_PIN_SEL	R/W	VBAT	0	LPC Master Pin Select.(F81967 only) 0 : Pin 111-118. 1 : Pin 17-21 and Pin 57-59.
2	LPC_M_EN	R/W	VBAT	0	0 : Disable LPC master. (F81967 only) 1 : Enable LPC master.
1-0	ESPI_MAX_ FREQ_SEL	R/W	VBAT	00	00 : eSPI ferquency capability is 20MHz. 01 : eSPI ferquency capability is 25MHz. 10 : eSPI ferquency capability is 33MHz. 11 : eSPI ferquency capability is 50MHz.

5.1.23 TSI/MXM Pin Select Register — Index 2Bh (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7-6	MXM_SDA_SEL	R/W	VBAT	0	MXM SDA Pin Select 00 : Select pin 68 as SDA. 01 : Select pin 62 as SDA. 10 : Select pin 71 as SDA. 11 : Select pin 55 as SDA.
5-4	MXM_SCL_SEL	R/W	VBAT	0	MXM SCL Pin Select 00 : Select pin 67 as SCL. 01 : Select pin 61 as SCL. 10 : Select pin 76 as SCL. 11 : Select pin 54 as SCL.
3-2	TSI_SDA_SEL	R/W	VBAT	0	TSI SDA Pin Select 00 : Select pin 68 as SDA. 01 : Select pin 62 as SDA. 10 : Select pin 71 as SDA. 11 : Select pin 55 as SDA.
1-0	TSI_SCL_SEL	R/W	VBAT	0	TSI SCL Pin Select 00 : Select pin 67 as SCL. 01 : Select pin 61 as SCL. 10 : Select pin 76 as SCL. 11 : Select pin 54 as SCL.

5.1.24 I2C Pin Select Register — Index 2Bh (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	R/W	VBAT	0	Dummy register for future use.
3-2	I2C_SDA_SEL	R/W	VBAT	0	I2C SDA Pin Select 00 : Select pin 68 as SDA. 01 : Select pin 62 as SDA. 10 : Select pin 71 as SDA. 11 : Select pin 55 as SDA.
1-0	I2C_SCL_SEL	R/W	VBAT	0	I2C SCL Pin Select 00 : Select pin 67 as SCL. 01 : Select pin 61 as SCL. 10 : Select pin 76 as SCL. 11 : Select pin 54 as SCL.

5.1.25 ERP Clock Fine Tune Count High Byte With A Period Register — Index 2Bh (CLK_TUNE_PORG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7	CLK_TUNE_ PERIOD	R/W	VBAT	3h	This bit is set when CLK_TUNE is set and auto clear after internal 20μs timer expires.
6-4	Reserved	-	-	-	Reserved.
3-0	CLK_TUNE_ CNT [11:8]	R/W	VBAT	3h	CLK_TUNE_CNT is counted by accurate 48MHz for 20μs. The error is used to program CLK_TUNE_DIV for ErP 10Hz clock fine tune.

5.1.26 Multi Function Select Register 5 — Index 2Ch (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	R/W	VBAT	-	Dummy register for future use.
4	GPIO04_EN	R/W	VBAT	0	SLP_SUS#/GPIO04 Function Select. 0: SLP_SUS#. 1: GPIO04.
3	GPIO03_EN	R/W	VBAT	1	SUS_ACK#/GPIO03 Function Select. 0: SUS_ACK#. 1: GPIO03. This bit has no effect if SDA3_PIN_EN is set.
2	GPIO02_EN	R/W	VBAT	1	SUS_WARN#/GPIO02 Function Select. 0: SUS_WARN#. 1: GPIO02. This bit has no effect if SCL3_PIN_EN is set.
1	GPIO01_EN	R/W	VBAT	0	ERP_CTRL1#/GPIO01 Function Select. 0: ERP_CTRL1#. 1: GPIO01.
0	GPIO00_EN	R/W	VBAT	0	ERP_CTRL0#/GPIO00 Function Select. 0: ERP_CTRL0#. 1: GPIO00.

5.1.27 Enable I2C Pin Register — Index 2Ch (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	SMBUS_EN	R/W	VBAT	0	Set “1” to enable pin 61’s SCL and pin 62’s SDA.
6	SDA3_PIN_EN	R/W	VBAT	0	Set “1” to enable pin 55’s SDA.
5	SDA2_PIN_EN	R/W	VBAT	0	Set “1” to enable pin 71’s SDA
4	SDA0_PIN_EN	R/W	VBAT	0	Set “1” to enable pin 68’s SDA
3	Reserved	R/W	VBAT	0	Dummy register for future use.
2	SCL3_PIN_EN	R/W	VBAT	0	Set “1” to enable pin 54’s SCL

1	SCL2_PIN_EN	R/W	VBAT	0	Set “1” to enable pin 76’s SCL
0	SCL0_PIN_EN	R/W	VBAT	0	Set “1” to enable pin 67’s SCL

5.1.28 Multi Function Select Register 6 — Index 2Ch (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_EN	R/W	VBAT	0	RSMRST#/GPIO27 Function Select. 0: RSMRST#. 1: GPIO27.
6	GPIO26_EN	R/W	VBAT	0	PWROK/GPIO26 Function Select. 0: PWROK. 1: GPIO26.
5	GPIO25_EN	R/W	VBAT	0	PSON#/GPIO25 Function Select. 0: PSON#. 1: GPIO25.
4	GPIO24_EN	R/W	VBAT	0	S3#/GPIO24 Function Select. 0: S3#. 1: GPIO24.
3	GPIO23_EN	R/W	VBAT	0	PWSOUT#/GPIO23 Function Select. 0: PWSOUT#. 1: GPIO23.
2	GPIO22_EN	R/W	VBAT	0	PSIN#/GPIO22 Function Select. 0: PSIN#. 1: GPIO22.
1	GPIO21_EN	R/W	VBAT	0	ATXPG/GPIO21 Function Select. 0: ATXPG. 1: GPIO21.
0	GPIO20_EN	R/W	VBAT	0	ALERT#/GPIO20 Function Select. 0: ALERT#. 1: GPIO20. This bit has no effect if SCL2_PIN_EN is set.

5.1.29 Multi Function Select Register — Index 2Ch (CLK_TUNE_PROG_EN = 0, BANK_PROG_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7	GPIO97_EN	R/W	VBAT	0	SLCT/GPIO97 Function Select. 0: SLCT. 1: GPIO97. This bit has no effect if FANIN3_EN is set.

6	GPIO96_EN	R/W	VBAT	0	FANIN2/GPIO96 Function Select. 0: FANIN2. 1: GPIO96.
5	GPIO95_EN	R/W	VBAT	0	FANIN1/GPIO95 Function Select. 0: FANIN1. 1: GPIO95.
4	GPIO94_EN	R/W	VBAT	1	MCLK/GPIO94 Function Select. 0: MCLK. 1: GPIO94. This bit has no effect if SMBUS_EN is set.
3	GPIO93_EN	R/W	VBAT	1	MDATA/GPIO93 Function Select. 0: MDATA. 1: GPIO93. This bit has no effect if SMBUS_EN is set.
2	GPIO92_EN	R/W	VBAT	0	GA20/GPIO92 Function Select. 0: GA20. 1: GPIO92.
1	GPIO91_EN	R/W	VBAT	0	KBRST#/GPIO91 Function Select. 0: KBRST#. 1: GPIO91.
0	GPIO90_EN	R/W	VBAT	0	LDRQ#/GPIO90 Function Select. 0: LDRQ#. 1: GPIO90.

5.1.30 ERP Clock Fine Tune Count Low Byte With A Period Register — Index 2Ch (CLK_TUNE_PORG_EN = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	CLK_TUNE_ CNT [7:0]	R/W	VBAT	0h	CLK_TUNE_CNT is counted by accurate 48MHz for 20μs. The error is used to program CLK_TUNE_DIV for ErP 10Hz clock fine tune.

5.1.31 Wakeup Control Register — Index 2Dh

Bit	Name	R/W	Reset	Default	Description
7	CLK_Source_SEL	R/W	VBAT	0	Clock source is from 0: CLKIN pin. 1: PCICLK pin.

<table>
<tr><td>6</td><td>3VSB_HYS_DIS</td><td>R/W</td><td>VBAT</td><td>0</td><td>0: Enable RSMRST# 3VSB power good detection hysteresis.
1: Disable RSMRST# 3VSB power good detection hysteresis.</td><td rowspan="2">There are 4 combinations for RSMRST# 3VSB power good level
{3VSB_HYS_DIS, 3VSB_PG_LVL}
00: 3.0V/2.9V
01: 2.8V/2.5V
10: 3.0V/3.0V
11: 2.8V/2.8V
※ Rising/Falling Voltage</td></tr>
<tr><td>5</td><td>3VSB_PG_LVL</td><td>R/W</td><td>VBAT</td><td>1</td><td>RSMRST# 3VSB power good level selection.</td></tr>
<tr><td>4</td><td>KEY_SEL_ADD</td><td>R/W</td><td>VBAT</td><td>0</td><td colspan="2">Refer to KEY_SEL.</td></tr>
<tr><td>3</td><td>WAKEUP_EN</td><td>R/W</td><td>VBAT</td><td>1</td><td colspan="2">0: disable KB/Mouse wakeup function.
1: enable KB/Mouse wakeup function.</td></tr>
<tr><td>2-1</td><td>KEY_SEL</td><td>R/W</td><td>VBAT</td><td>00</td><td colspan="2">Select the keyboard wakeup key. Accompany with KEY_SEL_ADD, there are several key select as list
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wake Key</th></tr>
<tr><td>0</td><td>00</td><td>Ctrl + Esc</td></tr>
<tr><td>0</td><td>01</td><td>Ctrl + F1</td></tr>
<tr><td>0</td><td>10</td><td>Ctrl + Space</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup Key</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power Key</td></tr>
<tr><td>1</td><td>10</td><td>Ctrl + Alt + Space</td></tr>
<tr><td>1</td><td>11</td><td>Space</td></tr>
</table></td></tr>
<tr><td>0</td><td>MO_SEL</td><td>R/W</td><td>VBAT</td><td>0</td><td colspan="2">Select the mouse wakeup key.
0: Wakeup by mouse clicking.
1: Wakeup by mouse clicking or movement.</td></tr>
</table>

5.2 Multifunction Function Register Mapping Table

There are four banks for the configuration registers. Program index 27h bit3,2 and 0 to select the corresponding bank:

BANK0 → 0x27[3:2] = 00; 0x27[0] = 0
BANK1 → 0x27[3:2] = 01; 0x27[0] = 0
BANK2 → 0x27[3:2] = 10; 0x27[0] = 0
BANK3 → 0x27[3:2] = 11; 0x27[0] = 0

5.2.1 Multi Function Register Mapping For Parallel Port (LPT)

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN102	FANIN3/SLCT/GPIO97	SLCT	1. Select BANK0 2. 0x28[5] = 0 3. Select BANK1 4. 0x28[4] = 0 5. 0x2b[2] = 0
PIN103	GPIO70/PE/FANCTL3/PWM_DAC3	PE	
PIN104	GPIO71/BUSY	BUSY	
PIN105	GPIO72/ACK#	ACK#	
PIN106	GPIO73/SLIN#	SLIN#	
PIN107	GPIO74/SPI_MISO/INIT#	INIT#	
PIN108	GPIO75/ SPI_MOSI/ERR#	ERR#	
PIN109	GPIO76/SPI_CLK/AFD#	AFD#	
PIN110	GPIO77/SPI_CS#/STB#	STB#	
PIN111	GPIO80/L#/PD0/M_LCLK	PD0	
PIN112	GPIO81/SEGA/PD1/M_SERRIQ	PD1	
PIN113	GPIO82/SEGB/PD2/M_LFRAME#	PD2	
PIN114	GPIO83/SEGC/PD3/M_LFRESET#	PD3	
PIN115	GPIO84/SEGD/PD4/M_LAD0	PD4	
PIN116	GPIO85/SEGE/PD5/ M_LAD1	PD5	
PIN117	GPIO86/SEGF/PD6/ M_LAD2	PD6	
PIN118	GPIO87/SEGG/PD7/ M_LAD3	PD7	

5.2.2 Multi Function Register Mapping For Hardware Monitor

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN71	BEEP/GPIO16/SDA	BEEP	1. Select BANK1 2. 0x2c[5] = 0 3. GPIO16_FUNC_SEL = 011
PIN76	ALERT#/GPIO20/SCL	ALERT#	1. Select BANK1 2. 0x2c[1] = 0 3. Select BANK2 4. 0x2c[0] = 0

PIN102	FANIN3/SLCT/ GPIO97	FANIN3	1. Select BANK0 2. 0x2b[1] = 1
PIN103	GPIO70/PE/FANCTL3/PWM_DAC3	FANCTL3	1. Select BANK0 2. 0x2b[0] = 1

5.2.3 Multi Function Register Mapping For KBC (PS/2 Mouse)

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN61	GPIO93/MDATA/SCL	MDATA	1. Select BANK1 2. 0x2c[7] = 0 3. Select BANK3 4. 0x2c[4:3] = 00
PIN62	GPIO94/MCLK/SDA	MCLK	

5.2.4 Multi Function Register Mapping For GPIO0x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN52	ERP_CTRL0#/GPIO00	GPIO00	1. Select BANK0 2. 0x2c[0] = 1
PIN53	ERP_CTRL1#/GPIO01	GPIO01	1. Select BANK0 2. 0x2c[1] = 1
PIN54	GPIO02/SUS_WARN#/SCL	GPIO02	1. Select BANK0 2. 0x2c[2] = 1 3. 0x27[3:2] = 01; 0x27[0] = 0 4. 0x2c[2] = 0
PIN55	GPIO03/SUS_ACK#/SDA	GPIO03	1. Select BANK0 2. 0x2c[3] = 1 3. Select BANK1 4. 0x2c[6] = 0
PIN56	SLP_SUS#/GPIO04	GPIO04	1. Select BANK0 2. 0x2c[4] = 1
PIN57 PIN58 PIN59	GPIO05/SOUT5/M_LAD1 GPIO06/SIN5//M_LAD2 GPIO07/RTS5#//M_LAD3	GPIO05 GPIO06 GPIO07	1. Select BANK0 2. 0x28[3:2] = 00

5.2.5 Multi Function Register Mapping For GPIO1x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN65	GPIO10/LED_VSB	GPIO10	1. GPIO10_FUNC_SEL = 000

PIN66	GPIO11/LED_VCC	GPIO11	1. GPIO11_FUNC_SEL = 000
PIN67	GPIO12/SCL/IRTX	GPIO12	1. Select BANK0 2. 0x28[4] = 0 3. Select BANK1 4. 0x2c[0] = 0 5. GPIO12_FUNC_SEL = 000
PIN68	GPIO13/SDA/IRRX	GPIO13	1. Select BANK0 2. 0x28[4] = 0 3. Select BANK1 4. 0x28[4] = 0 5. GPIO13_FUNC_SEL = 000
PIN69	GPIO14/ATX_AT_TRAP	GPIO14	1. GPIO14_FUNC_SEL = 000
PIN70	WDTRST#/GPIO15	GPIO15	1. GPIO15_FUNC_SEL = 000
PIN71	BEEP/GPIO16/SDA	GPIO16	1. Select BANK1 2. 0x2c[5] = 0 3. GPIO16_FUNC_SEL = 000
PIN72	PECI/GPIO17	GPIO17	1. Select BANK0 2. 0x28[7] = 0 3. GPIO17_FUNC_SEL = 000

5.2.6 Multi Function Register Mapping For GPIO2x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN76	ALERT#/GPIO20/SCL	GPIO20	1. Select BANK2 2. 0x2c[0] = 1 3. Select BANK1 4. 0x2c[1] = 0
PIN77	ATXPG_IN/GPIO21	GPIO21	1. Select BANK2 2. 0x2c[1] = 1
PIN78	PSIN#/GPIO22	GPIO22	1. Select BANK2 2. 0x2c[2] = 1
PIN79	PWSOUT#/GPIO23	GPIO23	1. Select BANK2 2. 0x2c[3] = 1
PIN80	S3#/GPIO24	GPIO24	1. Select BANK2 2. 0x2c[4] = 1
PIN81	PS_ON#/GPIO25	GPIO25	1. Select BANK2 2. 0x2c[5] = 1
PIN82	PWROK/GPIO26	GPIO26	1. Select BANK2

			2. 0x2c[6] = 1
PIN83	RSMRST#/GPIO27	GPIO27	1. Select BANK2 2. 0x2c[7] = 1

5.2.7 Multi Function Register Mapping For GPIO3x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN36	GPIO30/DCD3#	GPIO30	1. Select BANK0 2. 0x29[5:4] = 00
PIN37	GPIO31/RI3#	GPIO31	
PIN38	GPIO32/CTS3#	GPIO32	
PIN39	GPIO33/DTR3#	GPIO33	
PIN40	GPIO34/RTS3#	GPIO34	
PIN41	GPIO35/DSR3#	GPIO35	
PIN42	GPIO36/SOUT3	GPIO36	
PIN43	GPIO37/SIN3	GPIO37	

5.2.8 Multi Function Register Mapping For GPIO4x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN44	GPIO40/DCD4#	GPIO40	1. Select BANK0 2. 0x29[7:6] = 00
PIN45	GPIO41/RI4#	GPIO41	
PIN46	GPIO42/CTS4#	GPIO42	
PIN47	GPIO43/DTR4#	GPIO43	
PIN48	GPIO44/RTS4#	GPIO44	
PIN49	GPIO45/DSR4#	GPIO45	
PIN50	GPIO46/SOUT4	GPIO46	
PIN51	GPIO47/SIN4	GPIO47	

5.2.9 Multi Function Register Mapping For GPIO5x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN9	GPIO50/RTS6#/SEGC	GPIO50	1. 0x27[1] = 0 2. Select BANK0 3. 0x28[1:0] = 00 4. Select BANK1
PIN10	GPIO51/SIN6/SEGE	GPIO51	
PIN11	GPIO52/ SOUT6/SEGB	GPIO52	
PIN12	GPIO53/ DCD6#/SEGG	GPIO53	

PIN13	GPIO54/SPI_MISO/RI6#	GPIO54	5. 0x28[4] = 0
PIN14	GPIO55/ SPI_MOSI/CTS6#	GPIO55	
PIN15	GPIO56/SPI_CLK/DTR6#	GPIO56	
PIN16	GPIO57/SPI_CS#/DSR6#	GPIO57	

5.2.10 Multi Function Register Mapping For GPIO6x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN17	GPIO60/DCD5#/ M_LCLK	GPIO60	1. Select BANK0 2. 0x28[3:2] = 00
PIN18	GPIO61//RI5#/ M_SERRIQ	GPIO61	
PIN19	GPIO62/CTS5#/ M_LFRAME#	GPIO62	
PIN20	GPIO63/DTR5#/ M_LFRESET#	GPIO63	
PIN21	GPIO64//DSR5#/ M_LAD0	GPIO64	
PIN74	PME#/GPIO65	GPIO65	1. Select BANK0 2. 0x2b[5] = 1
PIN86	DPWROK/GPIO66	GPIO66	1. Select BANK0 2. 0x2b[6] = 1
PIN87	S5#/GPIO67	GPIO67	1. Select BANK0 2. 0x2b[7] = 1

5.2.11 Multi Function Register Mapping For GPIO7x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN103	GPIO70/PE/FANCTL3/PWM_DAC3	GPIO70	1. Select BANK0 2. 0x28[5] = 1 3. 0x2b[0] = 0
PIN104	GPIO71/BUSY	GPIO71	1. Select BANK0 2. 0x28[5] = 1
PIN105	GPIO72/ACK#	GPIO72	
PIN106	GPIO73/SLIN#	GPIO73	
PIN107	GPIO74/SPI_MISO/INIT#	GPIO74	
PIN108	GPIO75/ SPI_MOSI/ERR#	GPIO75	
PIN109	GPIO76/SPI_CLK/AFD#	GPIO76	
PIN110	GPIO77/SPI_CS#/STB#	GPIO77	

5.2.12 Multi Function Register Mapping For GPIO8x

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN111	GPIO80/L#/PD0/M_LCLK	GPIO80	1. Select BANK0 2. 0x28[5] = 1 3. 0x28[6] = 0
PIN112	GPIO81/SEGA/PD1/M_SERRIQ	GPIO81	
PIN113	GPIO82/SEGB/PD2/M_LFRAME#	GPIO82	
PIN114	GPIO83/SEGC/PD3/M_LFRESET#	GPIO83	
PIN115	GPIO84/SEGD/PD4/M_LAD0	GPIO84	
PIN116	GPIO85/SEGE/PD5/ M_LAD1	GPIO85	
PIN117	GPIO86/SEGF/PD6/ M_LAD2	GPIO86	
PIN118	GPIO87/SEGG/PD7/ M_LAD3	GPIO87	

5.2.13 Multi Function Register Mapping For WDT

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN70	WDTRST#/GPIO15	WDTRST#	1. GPIO15_FUNC_SEL = 110

5.2.14 Multi Function Register Mapping For ERP, LED

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN52	ERP_CTRL0#/GPIO00	ERP_CTRL0#	1. Select BANK0 2. 0x2c[0] = 0
PIN53	ERP_CTRL1#/GPIO01	ERP_CTRL1#	1. Select BANK0 2. 0x2c[1] = 0
PIN54	GPIO02/SUS_WARN#/SCL	SUS_WARN#	1. Select BANK0 2. 0x2c[2] = 0 3. Select BANK1 4. 0x2c[2] = 0
PIN55	GPIO03/SUS_ACK#/SDA	SUS_ACK#	1. Select BANK0 2. 0x2c[3] = 0 3. Select BANK1 4. 0x2c[6] = 0
PIN56	SLP_SUS#/GPIO04	SLP_SUS#	1. Select BANK0 2. 0x2c[4] = 0
PIN86	DPWROK/GPIO66	DPWROK	1. Select BANK0 2. 0x2b[6] = 0
PIN65	GPIO10/LED_VSB	LED_VSB	1. GPIO10_FUNC_SEL = 101

PIN66	GPIO11/LED_VCC	LED_VCC	1. GPIO11_FUNC_SEL = 100
PIN77	ATXPG_IN/GPIO21	ATXPG_IN	1. Select BANK2 2. 0x2c[1] = 0
PIN78	PWSIN#/GPIO22	PWSIN#	1. Select BANK2 2. 0x2c[2] = 0
PIN79	PWSOUT#/GPIO23	PWSOUT#	1. Select BANK2 2. 0x2c[3] = 0
PIN80	S3#/GPIO24	S3#	1. Select BANK2 2. 0x2c[4] = 0
PIN81	PS_ON#/GPIO25	PS_ON#	1. Select BANK2 2. 0x2c[5] = 0
PIN82	PWROK/GPIO26	PWOK	1. Select BANK2 2. 0x2c[6] = 0
PIN83	RSMRST#/GPIO27	RSMRST#	1. Select BANK2 2. 0x2c[7] = 0
PIN87	S5#/GPIO67	S5#	1. Select BANK0 2. 0x2b[7] = 0

5.2.15 Multi Function Register Mapping For IR

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN67 PIN68	GPIO12/SCL/IRTX GPIO13/SDA/IRRX	IRTX IRRX	1. Select BANK0 2. 0x28[4] = 1 3. Select BANK1 4. 0x2c[0] = 0; 0x2c[4] = 0

5.2.16 Multi Function Register Mapping For I2C

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN61 PIN62	GPIO93/MDATA/SCL GPIO94/MCLK/SDA	SCL SDA	1. Select BANK1 2. 0x2c[7] = 1
PIN71 PIN76	BEEP/GPIO16/SDA ALERT#/GPIO20/SCL	SDA SCL	1. Selet BANK1 2. 0x2c[5] = 1; 0x2c[1] = 1

5.2.17 Multi Function Register Mapping For UART 1 & UART 2

UART 1 & 2 are pure pins.

5.2.18 Multi Function Register Mapping For UART 3

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN36	GPIO30/DCD3#	DCD3#	1. Select BANK0 2. 0x29[5:4] = 00: GPIO function 01: Only SIN3/SOUT3 10: Only SIN3/SOUT3/RTS3# 11: Full UART
PIN37	GPIO31/RI3#	RI3#	
PIN38	GPIO32/CTS3#	CTS3#	
PIN39	GPIO33/DTR3#	DTR3#	
PIN40	GPIO34/RTS3#	RTS3#	
PIN41	GPIO35/DSR3#	DSR3#	
PIN42	GPIO36/SOUT3	SOUT3	
PIN43	GPIO37/SIN3	SIN3	

5.2.19 Multi Function Register Mapping For UART 4

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN44	GPIO40/DCD4#	DCD4#	1. Select BANK0 2. 0x29[7:6] = 00: GPIO function 01: Only SIN4/SOUT4 10: Only SIN4/SOUT4/RTS4# 11: Full UART
PIN45	GPIO41/RI4#	RI4#	
PIN46	GPIO42/CTS4#	CTS4#	
PIN47	GPIO43/DTR4#	DTR4#	
PIN48	GPIO44/RTS4#	RTS4#	
PIN49	GPIO45/DSR4#	DSR4#	
PIN50	GPIO46/SOUT4	SOUT4	
PIN51	GPIO47/SIN4	SIN4	

5.2.20 Multi Function Register Mapping For UART 5

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN17	GPIO60/DCD5#/M_LCLK	DCD5#	1. Select BANK0 2. 0x28[3:2] = 00: GPIO function 01: Only SIN5/SOUT5 10: Only SIN5/SOUT5/RTS5# 11: Full UART
PIN18	GPIO61/RI5#/M_SERIRQ	RI5#	
PIN19	GPIO62/CTS5#/M_LFRAME#	CTS5#	
PIN20	GPIO63/DTR5#/M_LRESET#	DTR5#	
PIN21	GPIO64//DSR5#/M_LAD0	DSR5#	
PIN57	GPIO05/SOUT5/M_LAD1	SOUT5	
PIN58	GPIO06/SIN5/M_LAD2	SIN5	
PIN59	GPIO07/RTS5#/M_LAD3	RTS5#	

5.2.21 Multi Function Register Mapping For UART 6

PIN No.	PIN FULL NAME	PIN SELECT	CONFIGURE REGISTER PROGRAM GUIDE
PIN9	GPIO50/RTS6#/SEGC	RTS6#	1. Select BANK0 2. 0x28[1:0] = 00: GPIO function 01: Only SIN6/SOUT6 10: Only SIN6/SOUT6/RTS6# 11: Full UART
PIN10	GPIO51/SIN6/SEGE	SIN6	
PIN11	GPIO52/ SOUT6/SEGB	SOUT6	
PIN12	GPIO53/ DCD6#/SEGG	DCD6#	
PIN13	GPIO54/SPI_MISO/RI6#	RI6#	
PIN14	GPIO55/ SPI_MOSI/CTS6#	CTS6#	
PIN15	GPIO56/SPI_CLK/DTR6#	DTR6#	
PIN16	GPIO57/SPI_CS#/DSR6#	DSR6#	

5.3 Parallel Port Device Configuration Registers (LDN CR03)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Parallel Port Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	0	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	1
74	DMA Channel Select Register	-	-	-	0	-	0	1	1
F0	PRT Mode Select Register	1	1	0	0	0	0	1	0

5.3.1 Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	PRT_EN	R/W	LRESET#	1	0: disable Parallel Port. 1: enable Parallel Port.

5.3.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of Parallel Port base address.

5.3.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	78h	The LSB of Parallel Port base address.

5.3.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELPRTIRQ	R/W	LRESET#	7h	Select the IRQ channel for Parallel Port.

5.3.5 DMA Channel Select Register — Index 74h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4	ECP_DMA_MODE	R/W	LRESET#	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	-	Reserved.
2-0	SELPRTDMA	R/W	LRESET#	011	Select the DMA channel for Parallel Port.

5.3.6 PRT Mode Select Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	SPP_IRQ_MODE	R/W	LRESET#	1	Interrupt mode in non-ECP mode. 0: Level mode. 1: Pulse mode.
6-3	ECP_FIFO_THR	R/W	LRESET#	1000	ECP FIFO threshold.
2-0	PRT_MODE	R/W	LRESET#	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

5.4 Hardware Device Configuration Registers (LDN CR04)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

5.4.1 Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	HM_EN	R/W	LRESET#	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

5.4.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	02h	The MSB of Hardware Monitor base address.

5.4.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	95h	The LSB of Hardware Monitor base address.

5.4.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELHMIRQ	R/W	LRESET#	0	Select the IRQ channel for Hardware Monitor.

5.4.5 Hardware Monitor Configuration Setting Registers (Accessed by LPC and I2C)

5.4.6 Hardware Monitor General Setting

Register 0x[HEX]	Register Name	Default Value MSB							LS B
01	Hardware Monitor and Standby Mode Register	-	-	-	-	-	0	1	1
02	Case Open, Alert, OVT Mode Register	0	0	0	0	0	0	0	0
03	Case Open Status Register	0	0	0	0	0	0	0	0
04	EN VBAT Monitoring & Monitor HWM Value at S3 Register	0	0	0	0	0	0	0	0
05	Temperature is Active Under S3 Control & Debug Port for Temperature Out Register	0	0	0	0	-	0	0	0
07	XM Address Register0	0	1	0	0	1	0	1	0

5.4.7 Hardware Monitor and Standby Mode Register — Index 01h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	0h	-	-	Reserved
2	POWER_DOWN	R/W	5VSB	0	Hardware monitor function power down function.
1	FAN_START	R/W	5VSB	1	1: enable startup of fan monitoring operations. 0: Put the part in the standby mode.
0	V_T_START	R/W	5VSB	1	1: enable startup of temperature and voltage monitoring operations 0: Put the part in the standby mode.

5.4.8 Case Open, Alert, OVT Mode Register — Index 02h

Bit	Name	R/W	Reset	Default	Description
7	TSI_RST_SEL	R/W	5VSB	0	0: MXM/TSI/PECI enable registers reset by LRESET#. 1: MXM/TSI/PECI enable registers reset by VDD3VOK. Affected registers are MXM_EN, TSI_EN and PECI_EN.
6	CASE_BEEP_EN	R/W	5VSB	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.
5-4	OVT_MODE	R/W	5VSB	0	00: The OVT# will be low active level mode. 01: The OVT# will be low pulse mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	Reserved	R/W	5VSB	0	Reserved for future use.
2	CASE_SMI_EN	R/W	5VSB	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	5VSB	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

5.4.9 Case Open Status Register — Index 03h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	R/W	-	0	Reserved
0	CASE_STS	R/W	VBAT	0	Case open event status, write 1 to clear if case open event cleared.

5.4.10 EN VBAT Monitoring & Monitor HWM Value at S3 Register— Index 04h

Bit	Name	R/W	Reset	Default	Description
7	VBAT_MON_DIS	R/W	5VSB	0	0: Enable VBAT monitoring. 1: Disable VBAT monitoring.
6-1	Reserved	R/W	5VSB	0	Reserved registers.
0	HM_S3_EN	R/W	5VSB	0	0: Hardware Monitor is in-active in S3 state. 1: Hardware Monitor is active in S3 state.

5.4.11 Temperature is Active Under S3 Control & Debug Port for Temperature Out Register — Index 05h

Bit	Name	R/W	Reset	Default	Description
7	MXM_S3_EN	R/W	5VSB	0	0: MXM is in-active in S3 state. 1: MXM is active in S3 state.
6	TSI_S3_EN	R/W	5VSB	0	0: TSI is in-active in S3 state. 1: TSI is active in S3 state.
5	PECI_S3_EN	R/W	5VSB	0	0: PECI is in-active in S3 state. 1: PECI is active in S3 state.
4	TEMP_OUT_EN	R/W	5VSB	0	Set “1” to output temperature value via debug port 7-segment LED.
3	Reserved	-	-	-	Reserved
2-0	DPORT_TEMP_SEL	R/W	5VSB	0h	0h: Local Diode reading. 1h: Diode 1 reading. 2h: Diode 2 reading. 3h: Reserved. 4h: TSI reading. 5h: MXM reading. 6h: Reserved. 7h: PECI reading.

5.4.12 MXM Address Register — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-1	MXM_ADDR	R/W	5VSB	4Ah	Address sent for MXM protocol.
0	Reserved	-	-	-	Reserved

5.4.13 PECI/TSI/I2C Setting

Register 0x[HEX]	Register Name	Default Value MSB							LS B
08	TSI or IBEX Control Register	0	1	0	0	1	1	0	0
09	I2C Address Control Register	0	0	0	0	0	0	0	-
0A	PECI, TSI, IBEX, Beta Register	0	0	0	0	0	0	0	0
0B	PECI Address Select Register	0	0	0	0	-	-	-	0
0C	TCC Register	0	1	0	1	0	1	0	1
0D	TSI Offset Register	0	0	0	0	0	0	0	0
0E	MXM Offset Register	0	0	0	0	0	0	0	0
0F	Configuration Register	0	0	0	0	0	0	1	0

5.4.14 TSI or IBEX Address Register — Index 08h

Bit	Name	R/W	Reset	Default	Description
7-1	TSI_ADDR	R/W	5VSB	4Ch	AMD TSI or Intel IBEX slave address.
0	Reserved	-	-	-	Reserved

5.4.15 I2C Address Control Register — Index 09h

Bit	Name	R/W	Reset	Default	Description
7-1	SMBUS_ADDR	R/W	5VSB	0	Address sent by embedded SMBus master.
0	Reserved	R/W	-	0	Reserved

5.4.16 PECI, TSI, IBEX Beta Register — Index 0Ah

Bit	Name	R/W	Reset	Default	Description
7	BETA_EN2	R/W	5VSB	0	0: disable the T2 beta compensation. 1: enable the T2 beta compensation.
6	BETA_EN1	R/W	5VSB	0	0: disable the T1 beta compensation. 1: enable the T1 beta compensation.
5	MXM_BYTE _MODE	R/W	5VSB	0	0: MXM is accessed by block read protocol. 1: MXM is accessed by send byte / receive byte protocol.
4	MXM_EN	R/W	VDD3VOK LRESET#	0	0: Disable MXM access. 1: Enable MXM access.
3-2	VTT_SEL	R/W	5VSB	0	PECI (VTT) voltage selection. 00: VTT is 1.23V 01: VTT is 1.13V 10: VTT is 1.00V 11: VTT is 1.00V

1	TSI_EN	R/W	VDD3VOK LRESET#	0	0: Disable AMD TSI access. 1: Enable AMD TSI access.
0	PECI_EN	R/W	VDD3VOK LRESET#	0	0: Disable PECI access. 1: Enable PECI access.

5.4.17 PECI Address Select Register — Index 0Bh

Bit	Name	R/W	Reset	Default	Description
7-4	CPU_SEL	R/W	5VSB	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping () command to find the CPU address. 0001: CPU is in socket 0, i.e. PECI address is 30h. 0010: CPU is in socket 0, i.e. PECI address is 31h. 0100: CPU is in socket 0, i.e. PECI address is 32h. 1000: CPU is in socket 0, i.e. PECI address is 33h. Others are reserved.
3-1	Reserved	-	-	-	Reserved.
0	DOMAIN1_EN	R/W	5VSB	0	If the CPU is selected as dual core. Set this register 1 to read the temperature of domain1.

5.4.18 TCC Register — Index 0Ch

Bit	Name	R/W	Reset	Default	Description
7-0	TCC_TEMP	R/W	5VSB	55	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127°C.

5.4.19 TSI Offset Register — Index 0Dh

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_OFFSET	R/W	5VSB	0	This byte is used as the offset to be added to the CPU temperature reading of AMD_TSI. The range of this register is -128 ~ 127°C.

5.4.20 MXM Offset Register — Index 0Eh

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_OFFSET	R/W	5VSB	0	This byte is used as the offset to be added to the temperature reading of MXM. The range of this register is -128 ~ 127°C.

5.4.21 Configuration Register — Index 0Fh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1-0	DIG_RATE_SEL	R/W	5VSB	2	Reserved for Fintek use only

5.4.22 PECI Command Setting

Register 0x[HEX]	Register Name	Default Value MSB							LS B
40	PECI Configuration Register	0	1	-	-	0	1	0	0
41	PECI Master Control Register	-	-	-	0	-	0	0	0
42	PECI Master Status Register	-	-	-	-	-	-	-	-
43~4F	PECI Master DATA0~12 Register	0	0	0	0	0	0	0	0

5.4.23 PECI Configuration Register — Index 40h

Bit	Name	R/W	Reset	Default	Description
7	RDIAMSR_CMD_EN	R/W	5VSB	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR() command before a GetTemp() command.
6	C3_UPDATE_EN	R/W	5VSB	1	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR() is 0x82.
5-4	Reserved	R	-	-	Reserved
3	C3_PTEMP_EN	R/W	5VSB	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is 0x82.
2	C0_PTEMP_EN	R/W	5VSB	1	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	5VSB	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is 0x82.
0	C0_ALL0_EN	R/W	5VSB	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.

5.4.24 PECI Master Control Register — Index 41h

Bit	Name	R/W	Reset	Default	Description
7	PECI_CMD_START	W	5VSB	-	Write 1 to this bit to start a PECI command when using as a PECI master (PECI_PENDING must be set to 1).
6-5	Reserved	R	-	-	Reserved
4	PECI_PENDING	R/W	5VSB	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	-	Reserved

2-0	PECI_CMD	R/W	5VSB	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

5.4.25 PECI Master Status Register — Index 42h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	-	Reserved
2	ABORT_FCS	R/WC	5VSB	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	5VSB	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
0	PECI_FINISH	R/WC	5VSB	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

5.4.26 PECI Master DATA0 Register — Index 43h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA0	R/W	5VSB	0	For RdIAMSR(), RdPkgConfig() and WrPkgConfig() command, this byte represents "Host ID[7:1] & Retry[0]". Please refer to PECI interface specification for more detail.

5.4.27 PECI Master DATA1 Register — Index 44h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA1	R/W	5VSB	0	For RdIAMSR() , this byte represents "Processor ID". For RdPkgConfig() and WrPkgConfig(), this byte represents "Index". Please refer to PECI interface specification for more detail.

5.4.28 PECI Master DATA2 Register — Index 45h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA2	R/W	5VSB	0	For RdIAMSR(), this byte is the least significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the least significant byte of "Parameter". Please refer to PECI interface specification for more detail.

5.4.29 PECI Master DATA3 Register — Index 46h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA3	R/W	5VSB	0	For RdIAMSR(), this byte is the most significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the most significant byte of "Parameter". Please refer to PECI interface specification for more detail.

5.4.30 PECI Master DATA4 Register — Index 47h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA4	R/W	5VSB	0	For GetDIB() , this byte represents "Device Info" For GetTemp(), this byte represents the least significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte is "Completion Code". For WrPkgConfig(), this byte represents "DATA[7:0]"

5.4.31 PECI Master DATA5 Register — Index 48h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA5	R/W	5VSB	0	For GetDIB() , this byte represents "Revision Number" For GetTemp(), this byte represents the most significant byte of temperature. For RdIAMSR() and RdPkgConfig(), this byte represents "DATA[7:0]" For WrPkgConfig(), this byte represents "DATA[15:8]"

5.4.32 PECI Master DATA6 Register — Index 49h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA6	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[15:8]". For WrPkgConfig(), this byte represents "DATA[23:16]"

5.4.33 PECI Master DATA7 Register — Index 4Ah

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA7	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[23:16]". For WrPkgConfig(), this byte represents "DATA[31:24]"

5.4.34 PECI Master DATA8 Register — Index 4Bh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA8	R/W	5VSB	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[31:24]". For WrPkgConfig(), this byte represents "AW FCS"

5.4.35 PECI Master DATA9 Register — Index 4Ch

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA9	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[39:32]". For WrPkgConfig(), this byte represents "Completion Code"

5.4.36 PECI Master DATA10 Register — Index 4Dh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA10	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[47:40]".

5.4.37 PECI Master DATA11 Register — Index 4Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA11	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[55:48]".

5.4.38 PECI Master DATA12 Register — Index 4Fh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA12	R/W	5VSB	0	For RdIAMSR(), this byte represents "DATA[63:56]".

5.4.39 TSI/MXM Temperature

Register 0x[HEX]	Register Name	Default Value							
		MSB							LS B
50	TSI Temperature	-	-	-	-	-	-	-	-
51	High Byte MXM Temperature Reading Register	-	-	-	-	-	-	-	-
52	Low Byte MXM Temperature Reading Register	-	-	-	-	-	-	-	-
53	MXM Index Register	0	0	0	0	0	0	1	1
54~5B	SMBus Data 0~7	0	0	0	0	0	0	0	0
5C	Block Write Count Registe	0	0	0	0	0	0	0	0
5D	SMBUS Command Byte/TSI Command Byte	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

5E	SMBUS Status	0	0	0	0	0	0	0	1
5F	SMBUS Protocol Select	0	-	-	-	0	0	0	0

5.4.40 TSI Temperature – Index 50h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP	R/W	5VSB	-	This is the AMD TSI temperature reading.

5.4.41 High Byte MXM Temperature Reading Register — Index 51h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP0	R/W	5VSB	-	This is the high byte of MXM temperature reading. The raw MXM temperature is determined by: MXM_BYTE_MODE is “0”, it is {MXM_TEMP0 [0], MXM_TEMP1 [7:1]}. MXM_BYTE_MODE is “1”, it is MXM_TEMP0 [7:0].

5.4.42 Low Byte MXM Temperature Reading Register — Index 52h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP1	R/W	5VSB	-	This is the low byte of MXM temperature reading. This byte is not used if MXM_BYTE_MODE is “1”.

5.4.43 MXM Index Register — Index 53h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP_IDX	R/W	5VSB	3h	This byte is used for 1. Command sent for MXM protocol if MXM_BYTE_MODE is “0”. 2. Index sent for MXM protocol if MXM_BYTE_MODE is “1”.

5.4.44 SMBus Data 0 – Index 54h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA0	R/W	5VSB	8’h00	This is the first byte of the block read/write protocol.

5.4.45 SMBus Data 1 – Index 55h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA1	R/W	5VSB	8’h00	This is the second byte of the block read/write protocol.

5.4.46 SMBus Data 2 – Index 56h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA2	R/W	5VSB	8'h00	This is the third byte of the block read/write protocol.

5.4.47 SMBus Data 3 – Index 57h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA3	R/W	5VSB	8'h00	This is the 4th byte of the block read/write protocol.

5.4.48 SMBus Data 4 – Index 58h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA4	R/W	5VSB	8'h00	This is the 5th byte of the block read/write protocol.

5.4.49 SMBus Data 5 – Index 59h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA5	R/W	5VSB	8'h00	This is the 6th byte of the block read/write protocol.

5.4.50 SMBus Data 6 – Index 5Ah

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA6	R/W	5VSB	8'h00	This is the 7th byte of the block read/write protocol.

5.4.51 SMBus Data 7 – Index 5Bh

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA7	R/W	5VSB	8'h00	This is the 8th byte of the block read/write protocol.

5.4.52 Block Write Count Register – Index 5Ch

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	0	Reserved
3-0	BLOCK_WR_CNT	R/W	5VSB	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

5.4.53 SMBUS Command Byte/TSI Command Byte – Index 5Dh

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_CMD/TSI_CMD	R/W	5VSB	0/1	There are actual two bytes for this index. TSI_CMD_PROG select which byte to be programmed: 0: SMBUS_CMD, which is the command code for write byte/word, read byte/word, block write/read and process call protocol. 1: TSI_CMD, which is the command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

5.4.54 SMBUS Status – Index 5Eh

Bit	Name	R/W	Reset	Default	Description
7	ADC_PENDING	R/W	5VSB	0	Set 1 to pending auto TSI/MXM accessing. To use the SCL/ SDA as SMBUS master, set this bit to “1” first.
6	TSI_CMD_PROG	R/W	5VSB	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	5VSB	0	Kill the current SMBUS transfer and return the state machine to idle. It will set a fail status if the current transfer is not completed.
4	FAIL_STS	R	5VSB	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next SMBUS transfer.
3	SMBUS_ABT_ERR	R	5VSB	0	This is the arbitration lost status if SMBUS command is issued. Auto cleared by next SMBUS command.
2	SMBUS_TO_ERR	R	5VSB	0	This is the timeout status if SMBUS command is issued. Auto cleared by next SMBUS command.
1	SMBUS_NAC_ERR	R	5VSB	0	This is the NACK error status if SMBUS command is issued. Auto cleared by next SMBUS command.
0	SMBUS_ READY	R	5VSB	1	0: SMBUS transfer is in process. 1: Ready for next SMBUS command.

5.4.55 SMBUS Protocol Select – Index 5Fh

Bit	Name	R/W	Reset	Default	Description
7	SMBUS_START	W	-	0	Write “1” to trigger SMBUS transfer with the protocol specified by SMBUS_PROTOCOL.
6-4	Reserved	-	-	-	Reserved.

3-0	SMBUS_PROTOCOL	R/W	5VSB	0	Select what protocol if SMBUS transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: Reserved. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: read word. 1101b: block read. 1111b: Reserved Otherwise: reserved.

5.4.56 Temperature Related Register

Register 0x[HEX]	Register Name	Default Value MSB							LS B
60	Temperature PME# Enable Register	-	0	0	0	-	0	0	0
61	Temperature Interrupt Status Register	-	0	0	0	-	0	0	0
62	Temperature Real Time Status Register	-	0	0	0	-	0	0	0
63	Temperature BEEP Enable Register	-	0	0	0	-	0	0	0
64	T1 OVT and High Limit Temperature Select Register	0	0	0	0	0	0	0	0
66	OVT and Alert Output Enable Register 1	-	0	0	0	-	0	1	0
6B	Temperature Sensor Type Register	0	0	0	0	0	1	1	-
6C	TEMP1 Limit Hystersis Select Register	0	1	0	0	0	1	0	0
6D	TEMP2 and TEMP3 Limit Hystersis Select Register	-	-	-	-	0	1	0	0
6F	DIODE OPEN Status Register	-	-	-	-	-	-	-	-
7F	T1 Slope Adjust Register	-	-	-	-	0	0	0	0
70~8D	Temperature	-	-	-	-	-	-	-	-

5.4.57 Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	-	Reserved
6	EN_ T2_OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	EN_ T0_ OVT_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP0 exceeds OVT setting.
3	Reserved	R/W	-	-	Reserved

2	EN_ T2_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	EN_ T0_EXC_PME	R/W	5VSB	0	If set this bit to 1, PME# signal will be issued when TEMP0 exceeds high limit setting.

5.4.58 Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	-	Reserved
6	T2_OVT _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
5	T1_OVT _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
4	T0_OVT _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP0 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
3	Reserved	R/W	-	-	Reserved
2	T2_EXC _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
1	T1_EXC _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
0	T0_EXC _STS	R/W	3VCC	0	A one indicates TEMP0 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.

5.4.59 Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	-	Reserved
6	T2_OVT	R/W	3VCC	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	3VCC	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	T0_OVT	R/W	3VCC	0	Set when the TEMP0 exceeds the OVT limit. Clear when the TEMP0 is below the “OVT limit –hysteresis” temperature.
3	Reserved	R/W	-	-	Reserved

2	T2_EXC	R/W	3VCC	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	3VCC	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	T0_EXC	R/W	3VCC	0	Set when the TEMP0 exceeds the high limit. Clear when the TEMP0 is below the “high limit –hysteresis” temperature.

5.4.60 Temperature BEEP Enable Register — Index 63h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	EN_ T2_OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	EN_ T0_OVT_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP0 exceeds OVT limit setting.
3	Reserved	R/W	-	-	Reserved
2	EN_ T2_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	EN_ T0_EXC_BEEP	R/W	5VSB	0	If set this bit to 1, BEEP signal will be issued when TEMP0 exceeds high limit setting.

5.4.61 T1 OVT and High Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved
5-4	OVT_TEMP_SEL	R/W	5VSB	0	Select the source temperature for T1 OVT Limit. 0: Select T1 to be compared to Temperature 1 OVT Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 OVT Limit. 2: Select CPU temperature from AMD TSI or Intel PCH I2C to be compared to Temperature 1 OVT Limit. 3: Select the MAX temperature from Intel PCH I2C to be compared to Temperature 1 OVT Limit.
3-2	Reserved	-	-	0	Reserved

1-0	HIGH_ TEMP_SEL	R/W	5VSB	0	Select the source temperature for T1 High Limit. 0: Select T1 to be compared to Temperature 1 High Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 High Limit. 2: Select CPU temperature from AMD TSI or Intel PCH I2C to be compared to Temperature 1 High Limit. 3: Select the MAX temperature from Intel PCH I2C to be compared to Temperature 1 High Limit.

5.4.62 OVT and Alert Output Enable Register 1 — Index 66h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	-	-	Reserved
6	EN_T2_ALERT	R/W	5VSB	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R/W	5VSB	0	Enable temperature 1 alert event (asserted when temperature over high limit)
4	EN_T0_ALERT	R/W	5VSB	0	Enable temperature 0 alert event (asserted when temperature over high limit)
3	Reserved	R/W	-	-	Reserved
2	EN_T2_OVT	R/W	5VSB	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	5VSB	1	Enable over temperature (OVT) mechanism of temperature1.
0	EN_T0_OVT	R/W	5VSB	0	Enable over temperature (OVT) mechanism of temperature0.

5.4.63 Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	RO	-	0	Reserved
2	T2_MODE	R/W	5VSB	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	5VSB	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	-	-	-	Reserved

5.4.64 TEMP1 Limit Hystersis Select Register — Index 6Ch

Bit	Name	R/W	Reset	Default	Description
7-4	TEMP1_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

3-0	TEMP0_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

5.4.65 TEMP2 and TEMP3 Limit Hystersis Select Register — Index 6Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3-0	TEMP2_HYS	R/W	5VSB	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

5.4.66 DIODE OPEN Status Register — Index 6Fh

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	MXM_OPEN	R	3VCC	-	When MXM interface is enabled, “1” indicates the error of receiving NACK bit or a timeout occurred.
5	PECI_OPEN	R	3VCC	-	When PECI interface is enabled, “1” indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4	TSI_OPEN	R	3VCC	-	When TSI interface is enabled, “1” indicates the error of receiving NACK bit or a timeout occurred.
3	Reserved	-	-	-	Reserved
2	T2_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 2 is open or short
1	T1_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 1 is open or short
0	T0_DIODE_OPEN	R	3VCC	-	“1” indicates internal diode is open or short

5.4.67 Temperature — Index 70h- 8Dh

Address	Attribute	Reset	Default Value	Description
70h	R	3VCC/5VSB	--	Local Temperature reading. The unit of reading is 1°C.At the moment of reading this register.
71h	Reserved	--	--	Reserved
72h	R	3VCC/5VSB	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	Reserved	--	--	Reserved
74h	R	3VCC/5VSB	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75-79h	Reserved	--	--	Reserved
7Ah	R	3VCC/5VSB	-	The data of CPU temperature from digital interface after IIR filter. (Available if Intel IBX or AMD TSI interface is enabled)
7Bh	R	3VCC/5VSB	-	The raw data of PCH temperature from digital interface. (Only available if Intel IBX interface is enabled)
7Ch	R	3VCC	-	Reserved

7Dh	R	3VCC	-	Reserved
7Eh	R	3VCC/5VSB	-	The data of CPU temperature from digital interface after IIR filter. (Only available if PECI interface is enabled)
80h	R/W	5VSB	46h	Temperature sensor 1 OVT limit. The unit is 1°C.
81h	R/W	5VSB	3Ch	Temperature sensor 1 high limit. The unit is 1°C.
82h	R/W	5VSB	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	5VSB	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	5VSB	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	5VSB	55h	Temperature sensor 2 high limit. The unit is 1°C.
86-8Bh	--	--	-	Reserved
8C~8Dh	--	--	--	Reserved

5.4.68 T1 Slope Adjust Register — Index 7Fh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	T1_ADD	R/W	5VSB	0	This bit is the sign bit for T1 reading slope adjustment. See T1_SCALE below for detail.
2-0	T1_SCALE	R/W	-	0h	

T1_ADD	T1_SCALE	Slope
X	00	No adjustment
0	01	15/16
0	10	31/32
0	11	63/64
1	01	17/16
1	10	33/32
1	11	65/64

5.4.69 Voltage Setting

Register 0x[HEX]	Register Name	Default Value MSB							LS B
10	Voltage-Protect Shut Down Enable Register	0	0	0	0	0	0	0	0
11	Voltage-Protect Status Register	-	-	-	-	-	-	-	0
12	Voltage-Protect Configuration Register	-	-	-	-	0	1	1	0
14	VIN1 Over Voltage SMI Enable Register	0	0	0	0	0	0	0	0
15	VIN1 Over Voltage Status Register	0	0	0	0	0	0	0	0
16	Voltage1 Exceeds Real Time Status Register	-	-	-	-	-	-	0	-
17	VIN1 Over Voltage BEEP Enable Register	-	-	-	-	-	-	0	-
20~3A	Voltage Reading & Limit	-	-	-	-	-	-		
3F	Voltage Protection Power Good Select Register	-	-	-	-	-	-	-	0

5.4.70 Voltage-Protect Shut Down Enable Register — Index 10h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	0	Reserved.
6	V3_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for VIN3
5	V2_VP_EN	R/W	VBAT*	0	Voltage-Protect enable for VIN2
4-1	Reserved	-	-	0	Reserved
0	VCC_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for 3VCC

**OVP Enable bit is auto clear when OVP event occurs if OVP_MODE is "1" and ALARM_RESET_DIS is "0"*

5.4.71 Voltage-Protect Status Register — Index 11h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
0	OVP_EXC_STS	R/W	5VSB	0	This bit is set when OVP occurs. Write "1" to clear this bit.

5.4.72 Voltage-Protect Configuration Register — Index 12h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-2	PU_TIME	R/W	VBAT	2'h1	PS_ON# de-active time select in alarm mode of voltage protection. 00: PS_ON# tri-state 0.5 sec and then inverted of S3# when over voltage or under voltage occurred. 01: PS_ON# tri-state 1 sec and then inverted of S3# when over voltage or under voltage occurred. 10: PS_ON# tri-state 2 sec and then inverted of S3# when over voltage or under voltage occurred. 11: PSON# tri-state 4 sec and then inverted of S3# when over voltage or under voltage occurred.
1-0	VP_EN_DELAY	R/W	VBAT	2'h2	VP_EN_DELAY could set the delay time to start voltage protecting after VDD power is ok when OVP_MODE is 1. (OVP_MODE is strapped by RTS1# pin) 00: bypass 01: 50ms 10: 100ms 11: 200ms

5.4.73 VIN1 Over Voltage SMI Enable Register — Index 14h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved
1	V1_SMI_EN	R/W	5VSB	0	0: Disable V1 over voltage SMI. 1: Enable V1 over voltage SMI.
0	Reserved	-	-	0	Reserved

5.4.74 VIN1 Over Voltage Status Register — Index 15h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	0	Reserved
1	V1_ EXC _STS	R/WC	5VSB	0	This bit is set when V1_EXC is changed. Write “1” to clear this bit.
0	Reserved	-	-	0	Reserved

5.4.75 VIN 1 Exceeds Real Time Status Register — Index 16h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	-	Reserved
1	V1_EXC	R/WC	5VSB	0	VIN1 over limit real time status. It is set when VIN1 is over V1_HIGH_LIMIT and clear when VIN1 is under V1_HIGH_LIMIT. This bit is also used to assert BEEP when V1_BEEP_EN is set.
0	Reserved	--	-	-	Reserved

5.4.76 VIN1 Over Voltage BEEP Enable Register — Index 17h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	-	Reserved
1	V1_BEEP_EN	R/W	5VSB	0	VIN1 (Vcore) Beep event enable.
0	Reserved	--	-	-	Reserved

5.4.77 Voltage Protection Power Good Select Register — Index 3Fh

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	--	-	-	Reserved
0	OVP_RST_SEL	R/W	VBAT	0	0: OVP/UVP power good signal is 3VCCOK (3VCC > 2.8V) 1: OVP/UVP power good signal is PWROK. OVP/UVP function wont’ start detecting until power good.

5.4.78 Voltage Reading and Limit— Index 20h- 3Ah

Address	Attribute	Reset	Default Value	Description
20h	R	3VCC	-	3VCC reading. The unit of reading is 8mV.
21h	R	3VCC	-	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	R	3VCC	-	VIN2 reading. The unit of reading is 8mV.
23h	R	3VCC	-	VIN3 reading. The unit of reading is 8mV.
24h	R	3VCC	-	VIN4 reading. The unit of reading is 8mV.
25h	R	3VCC	-	VSB3V reading. The unit of reading is 8mV.
26h	R	3VCC	-	VBAT reading. The unit of reading is 8mV.
27h	R	3VCC	-	5VSB reading. The unit of reading is 8 mV. The 5VSB voltage to be monitored is internally divided by 3.
28h~2Ch	R	--	-	Reserved
2Dh	R	3VCC	-	FAN3 present fan duty reading
2Eh	R	3VCC	-	FAN2 present fan duty reading
2Fh	R	3VCC	-	FAN1 present fan duty reading
30h	R/W	VBAT	89h	3VCC under-voltage protection limit. The unit is 8mV
31h	R/W	VBAT	F2h	3VCC over-voltage protection limit. The unit is 8 mV
32~35h	R		FF	Reserved
36h	R/W	VBAT	E2h	VIN2 over-voltage limit (V5_OVV_LIMIT). The unit is 8mv.
37h	R/W	VBAT	E1h	VIN3 over-voltage limit (V6_OVV_LIMIT). The unit is 8mv.
38h	R/W	VBAT	83h	VIN2 under-voltage limit (V5_UVV_LIMIT). The unit is 8mv.
39h	R/W	VBAT	96h	VIN3 under-voltage limit (V6_UVV_LIMIT). The unit is 8mv.
3Ah	R/W	5VSB	FFh	VIN1 high limit. The unit is 8mv.

5.4.79 General Fan Control Setting

Register 0x[HEX]	Register Name	Default Value							
		MSB							LS B
90	FAN PME# Enable Register	-	-	-	-	-	0	0	0
91	FAN Interrupt Status Register	-	-	-	-	-	-	-	-
92	FAN Real Time Status Register	-	-	-	-	-	-	-	-
93	FAN BEEP# Enable Register	-	0	0	-	-	0	0	0
94	FAN Type Select Register	0	0	0	0	0	0	0	0
94	Fan1 Base Temperature (Tb) Register	0	0	0	0	0	1	0	1
95	FAN1 Temperature Adjustment (Ta) Rate Register	-	0	0	0	-	0	0	0
96	FAN Mode Select Register (FAN_PROG_SEL = 0)	0	0	0	1	0	1	0	1
96	FAN1 Temperature Adjustment Select register (FAN_PROG_SEL = 1)	-	-	-	-	-	0	0	0
97	FAN PWM Frequency Select & FANIN Filter Time Register (FAN_PROG_SEL = 0)	-	0	0	0	-	0	0	0
97	Faster FAN Filter Time Register (FAN_PROG_SEL = 1)	-	-	-	-	-	0	0	0

98	Auto FAN1 and FAN2 Boundary Hystersis Select Register	0	1	0	0	0	1	0	0
99	Auto FAN3 Boundary Hystersis Select Register	-	-	-	-	0	0	1	0
9A	Fan Control Register (FAN_PROG_SEL = 0)	0	0	0	0	0	0	0	0
9A	PWM Frequency Divisor Register (FAN_PROG_SEL = 1)	0	0	0	0	0	0	0	0
9B	Auto Fan Up Speed Update Rate Select Register	-	-	0	1	0	1	0	1
9B	Auto Fan Down Speed update Rate Select Register	0	0	0	1	0	1	0	1
9C	FAN1 and FAN2 Start Up Duty-cycle/Voltage	0	1	0	1	0	1	0	1
9D	FAN3 Start Up Duty-cycle/Voltage	-	-	-	-	0	1	0	1
9E	FAN Programmable Duty-cycle/Voltage Loaded After Power On	0/1	1	1	0/1	0/1	1	1	0/1
9F	Fan Fault Time Register	0	0	-	-	1	0	1	0

5.4.80 FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	-	Reserved
2	EN_FAN3_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt Set this bit 1 to enable PME# function for FAN3.
1	EN_FAN2_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for FAN2.
0	EN_FAN1_PME	R/W	5VSB	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for FAN1.

5.4.81 FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	-	Reserved
2	FAN3_ST	R/W	3VCC	-	This bit is set when the FAN3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_ST	R/W	3VCC	-	This bit is set when the FAN2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_ST	R/W	3VCC	-	This bit is set when the FAN1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

5.4.82 FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	--	-	-	Reserved
2	FAN3_EXC	R	3VCC	-	This bit set to high mean that FAN3 count can't meet the expected count over than SMI time (CR9F) or when duty not zero but fan stop over 3 sec.
1	FAN2_EXC	R	3VCC	-	This bit set to high mean that FAN2 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over 3 sec.
0	FAN1_EXC	R	3VCC	-	This bit set to high mean that FAN1 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over 3 sec.

5.4.83 FAN BEEP# Enable Register — Index 93h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	FULL_WITH_ T2_EN	R/W	5VSB	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_ T1_EN	R/W	5VSB	0	Set one will enable FAN to force full speed when T1 over high limit.
4	FULL_WITH_ T0_EN	R/W	5VSB	0	Set one will enable FAN to force full speed when T0 over high limit.
3	Reserved	-	-	-	Reserved
2	EN_FAN3_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.
1	EN_FAN2_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	5VSB	0	A one enables the corresponding interrupt status bit for BEEP.

5.4.84 FAN Type Select Register — Index 94h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved.
5-4	FAN3_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTL3 0: FANCTL3 is pull up by external resistor. 1: FANCTL3 is pull down by internal 100KΩ resistor.

3-2	FAN2_TYPE	R/W	3VCC	01	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTL2 0: FANCTL2 is pull up by external resistor. 1: FANCTL2 is pull down by internal 100KΩ resistor.
1-0	FAN1_TYPE	R/W	3VCC	01	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTL1 0: FANCTL1 is pull up by external resistor. 1: FANCTL1is pull down by internal 100KΩ resistor.

S: Register default values are decided by trapping.

5.4.85 Fan1 Base Temperature (Tb) Register – Offset 94h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	FAN1_BASE _TEMP	R/W	5VSB	0	This register is used to set the base temperature for FAN1 temperature adjustment. The FAN1 temperature is calculated according to the equation: TFAN1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG (Index AFh, bit 7) and FAN1_TEMP_SEL (Index AFh bit 1-0). Tb is this register, Ta is selected by FAN1_ADJ_SEL and Ct is selected by FAN1_TEMP_ADJ_ UP_RATE (Ctup) (Index 95h, bith 6-4)/ FAN1_TEMP_ADJ_ DN_RATE (Ctdn) (Index 95h, bith 2-0) To access this register, FAN_PROG_SEL (index 9F[7]) must set to "1".

5.4.86 FAN1 Temperature Adjustment (Ta) Rate Register — Index 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6-4	FAN1_TEMP_ADJ_ UP_RATE (Ctup)		5VSB	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3'h1: 1 h (Ct = 1) 3'h2: 2h (Ct= 1/2) 3'h3: 3h (Ct = 1/4) 3'h4: 4h (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to "1".
3	Reserved	-		-	Reserved

2-0	FAN1_TEMP_ADJ_DN_RATE (Ctdn)	R/W	5VSB	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3'h1: 1 h (Ct = 1) 3'h2: 2h (Ct= 1/2) 3'h3: 3h (Ct = 1/4) 3'h4: 4h (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to "1".

5.4.87 FAN Mode Select Register — Index 96h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved
5-4	FAN3_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xC6-0xCE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xC6-0xCE. 10: Manual mode fan control. User can write expected **RPM** count to 0xC2-0xC3, and F81962/F81964/F81966/F81967 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control. User can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xC3, and F81962/F81964/F81966/F81967 will output this desired duty or voltage to control fan speed.
3-2	FAN2_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xB6-0xBE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** (voltage) defined in 0xB6-0xBE. 10: Manual mode fan control. User can write expected **RPM** count to 0xB2-0xB3, and F81962/F81964/F81966/F81967 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F81962/F81964/F81966/F81967 will output this desired duty or voltage to control fan speed.

1-0	FAN1_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xA6-0xAE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expected **RPM** count to 0xA2-0xA3, and F81962/F81964/F81966/F81967 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F81962/F81964/F81966/F81967 will output this desired duty or voltage to control fan speed.

5.4.88 FAN1 Tempertaure Adjustment (Ta) Select Register — Index 96h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved
2-0	FAN1_ADJ_SEL	R/W	5VSB	0h	This selects which temperature to be used as Ta for Fan1 temperature adjustment. 000: PECI (CR7Eh) 001: T1 (CR72h) 010: T2 (CR74h) 011: T3 (CR76h) 100: IBEX/TSI CPU temperature (CR7Ah) 101:IBEX PCH temperature (CR7Bh). 110: IBEX MCH temperature (CR7Ch). 111: IBEX maximum temperature (CR7Dh). otherwise: Ta will be 0. To access this register FAN_PROG_SEL must set to “1”.

5.4.89 FAN PWM Frequency Select & FANIN Filter Time Register — Index 97h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved.
6	FAN3_PWM_FREQ_SEL_EX2	R/W	5VSB	0	{FAN3_PWM_FREQ_SEL_EX2, FAN3_PWM_FREQ_SEL_EX, FAN3_PWM_FREQ_SEL} are used to select FAN3 PWM frequency. 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: Programmable by PWM_CLK_DIV. The frequency is 1MHz/(256*(PWM_CLK_DIV+1))

5	FAN2_PWM_FREQ_SEL_EX2	R/W	5VSB	0	{FAN2_PWM_FREQ_SEL_EX2, FAN2_PWM_FREQ_SEL_EX, FAN2_PWM_FREQ_SEL} are used to select FAN2 PWM frequency. 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: Programmable by PWM_CLK_DIV. The frequency is 1MHz/(256*(PWM_CLK_DIV+1))
4	FAN1_PWM_FREQ_SEL_EX2	R/W	5VSB	0	{FAN1_PWM_FREQ_SEL_EX2, FAN1_PWM_FREQ_SEL_EX, FAN1_PWM_FREQ_SEL} are used to select FAN1 PWM frequency. 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: Programmable by PWM_CLK_DIV. The frequency is 1MHz/(256*(PWM_CLK_DIV+1))
3	Reserved	-	5VSB	-	Reserved
2	FAN3_FLT_SEL	R/W	5VSB	0	Select the FANIN3 Filter time. 0: 640us/1280us depending on output duty. 1: 320us/640us depending on output duty.
1	FAN2_FLT_SEL	R/W	5VSB	0	Select the FANIN2 Filter time. 0: 640us/1280us depending on output duty. 1: 320us/640us depending on output duty.
0	FAN1_FLT_SEL	R/W	5VSB	0	Select the FANIN1 Filter time. 0: 640us/1280us depending on output duty. 1: 320us/640us depending on output duty.

5.4.90 Faster FAN Filter Time Register — Index 97h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-		-	Reserved
2	FAN3_FLT_FAST	R/W	5VSB	0	Set “1” to reduce filter time for FANIN3. 0: As controlled by FAN3_FLT_SEL and FANCTRL3 duty. 1: 640us/1280us reduce to 400us/1040us; 320us/640us reduce to 240us/560us.
1	FAN2_FLT_FAST	R/W	5VSB	0	Set “1” to reduce filter time for FANIN2. 0: As controlled by FAN2_FLT_SEL and FANCTRL2 duty. 1: 640us/1280us reduce to 400us/1040us; 320us/640us reduce to 240us/560us.
0	FAN1_FLT_FAST	R/W	5VSB	0	Set “1” to reduce filter time for FANIN1. 0: As controlled by FAN1_FLT_SEL and FANCTRL1 duty. 1: 640us/1280us reduce to 400us/1040us; 320us/640us reduce to 240us/560us.

5.4.91 Auto FAN1 and FAN2 Boundary Hystersis Select Register — Index 98h

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_HYS	R/W	5VSB	4h	Boundary hysteresis. (0~15°C). Segment will change when the temperature is over the boundary temperature and below the boundary deducts the hysteresis temperature.
3-0	FAN1_HYS	R/W	5VSB	4h	Boundary hysteresis. (0~15°C). Segment will change when the temperature is over the boundary temperature and below the boundary deducts the hysteresis temperature.

5.4.92 Auto FAN3 Boundary Hystersis Select Register — Index 99h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	FAN3_HYS	R/W	5VSB	2h	Boundary hysteresis. (0~15°C). Segment will change when the temperature is over the boundary temperature and below the boundary deducts the hysteresis temperature.

5.4.93 Fan Control Register — Index 9Ah (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	0	Reserved.
6	FAN3_PWM_ FREQ_SEL_EX	R/W	5VSB	0	{FAN3_PWM_FREQ_SEL_EX2, FAN3_PWM_FREQ_SEL_EX, FAN3_PWM_FREQ_SEL} are used to select FAN3 PWM frequency. 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: Programmable by PWM_CLK_DIV. The frequency is 1MHz/(256*(PWM_CLK_DIV+1))
5	FAN2_PWM_ FREQ_SEL_EX	R/W	5VSB	0	{FAN2_PWM_FREQ_SEL_EX2, FAN2_PWM_FREQ_SEL_EX, FAN2_PWM_FREQ_SEL} are used to select FAN2 PWM frequency. 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: Programmable by PWM_CLK_DIV. The frequency is 1MHz/(256*(PWM_CLK_DIV+1))
4	FAN1_PWM_ FREQ_SEL_EX	R/W	5VSB	0	{FAN1_PWM_FREQ_SEL_EX2, FAN1_PWM_FREQ_SEL_EX, FAN1_PWM_FREQ_SEL} are used to select FAN1 PWM frequency. 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: Programmable by PWM_CLK_DIV. The frequency is 1MHz/(256*(PWM_CLK_DIV+1))

3	FAN3_MANU_ FLT_EN	R/W	5VSB	0	Set “1” to disable FANIN3 filter controlled by FANCTRL3 duty.
2	FAN3_MANU_ FLT_SEL	R/W	5VSB	0	Select FANIN3 filter time when FAN3_MANU_FLT_EN is set. 0: 640us/1280us. 1: 320us/640us.
1-0	Reserved	--	-	0	Reserved

5.4.94 PWM Frequency Divisor Register — Index 9Ah (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	PWM_CLK_ DIV	R/W	5VSB	0	Clock divisor for PWM output. Refer to FAN1_PWM_FREQ_SEL/FAN2_PWM_FREQ_SEL/ FAN3_PWM_FREQ_SEL for detail.

5.4.95 Auto Fan Up Speed Update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved.
5-4	FAN3_UP_RATE	R/W	5VSB	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_UP_RATE	R/W	5VSB	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_UP_RATE	R/W	5VSB	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

5.4.96 Auto Fan Down Speed update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	UP_DN_RATE_EN	R/W	5VSB	0	0: FAN down rate disable 1: FAN down rate enable Set this bit 1 to use different fan up/down rate. If this bit is not set to 1, the fan up/down rate will follow FAN_UP_RATE.

6	DIRECT_LOAD_EN	R/W	5VSB	0	0: Direct load disable 1: Direct load enable for manual duty mode
5-4	FAN3_DN_RATE	R/W	5VSB	01	FAN3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_DN_RATE	R/W	5VSB	01	FAN2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DN_RATE	R/W	5VSB	01	FAN1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

5.4.97 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_STOP _DUTY	R/W	5VSB	5h	When fan start, the FANCTL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FANCTL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP _DUTY	R/W	5VSB	5h	When fan start, the FANCTL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FANCTL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

5.4.98 FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	FAN3_STOP_ DUTY	R/W	5VSB	5h	When fan start, the FANCTL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FANCTL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

5.4.99 FAN PROGRAMMABLE DUTY-CYCLE/VOLTAGE LOADED AFTER POWER-ON — Index 9Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PROG_DUTY_VAL	R/W	5VSB	66h/FFh	This byte will be immediately loaded as Fan duty value after VDD is powered on if it has been programmed before shut down. Default value is powered on strapped by FAN_40_100. When this byte is programmed, FAN will initial load this value when power on.

5.4.100 Fan Fault Time Register — Index 9Fh

Bit	Name	R/W	Reset	Default	Description
7	FAN_PROG_SEL	R/W	5VSB	0	Set this bit to “1” will enable accessing registers of other bank.
6	FAN_MNT_SEL	R/W	5VSB	0	Set this bit to monitor a slower fan.
5-4	Reserved	-	-	-	Reserved
3-0	F_FAULT_TIME	R/W	5VSB	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can’t reach the fan expect count in time. The unit of this register is 1 second. The default value is 10 seconds. (Set to 0, means 1 seconds; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 9C-9Dh.

5.4.101 FAN1 Control Register – Index A0h~Afh

Register 0x[HEX]	Register Name	Default Value							
		MSB							LS B
A0	FAN1 count reading (MSB)	0	0	0	0	1	1	1	1
A1	FAN1 count reading (LSB)	1	1	1	1	1	1	1	1
A2	FAN1 expect speed count value (MSB)	0	0	0	0	0	0	0	0
A3	FAN1 expect speed count value (LSB)	1	0	0	0	0	0	0	0
A4	FAN1 full speed count reading (MSB)	0	0	0	0	0	0	1	1
A5	FAN1 full speed count reading (LSB)	1	1	1	1	1	1	1	1
A6	FAN 1 Boundary 1 Temperature Register	0	0	1	1	1	1	0	0
A7	FAN 1 Boundary 2 Temperature Register	0	0	1	1	0	0	1	0
A8	FAN 1 Boundary 3 Temperature Register	0	0	1	0	1	0	0	0
A9	FAN 1 Boundary 4 Temperature Register	0	0	0	1	1	1	1	0
AA	FAN1 Segment 1 Speed Count Register	1	1	1	1	1	1	1	1
AB	FAN1 Segment 2 Speed Count Register	1	1	0	1	1	0	0	1
AC	FAN1 Segment 3 Speed Count Register	1	0	1	1	0	0	1	0
AD	FAN1 Segment 4 Speed Count Register	1	0	0	1	1	0	0	1

AE	FAN1 Segment 5 Speed Count Register	1	0	0	0	0	0	0	0
AF	FAN1 Temperature Mapping Select	0	0	0	1	1	1	0	1

Address	Attribute	Reset	Default	Description
A0h	RO	3VCC	8'h0F	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	3VCC	8'hFF	FAN1 count reading (LSB).
A2h	R/W	5VSB	8'h00	RPM mode(CR96 bit0=0): FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. Duty mode(CR96 bit0=1): This byte is reserved byte.
A3h	R/W	5VSB	8'h80	RPM mode(CR96 bit0=0): FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit0=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	5VSB	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	5VSB	8'hFF	FAN1 full speed count reading (LSB).

5.4.102 VT 1 Boundary 1 Temperature Register – Index A6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP1	R/W	5VSB	3Ch (60°C)	The 1st boundary temperature: When temperature exceeds this boundary, expected FAN1 value will be loaded from segment 1 register (index AAh). When temperature is under this (boundary – hysteresis), expected FAN1 value will be loaded from segment 2 register (index ABh). This byte is 2's complement value ranging from -128°C ~ 127°C.

5.4.103 VT 1 Boundary 2 Temperature Register – Index A7

Bit	Name	R/W	Reset	Default	Description

7-0	BOUND2TMP1	R/W	5VSB	32h (50˚C)	The 2nd boundary temperature: When temperature exceeds this boundary, expected FAN1 value will be loaded from segment 2 register (index ABh). When temperature is under this (boundary – hysteresis), expected FAN1 value will be loaded from segment 3 register (index ACh). This byte is 2's complement value ranging from -128ºC ~ 127ºC.

5.4.104 VT 1 Boundary 3 Temperature Register– Index A8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP1	R/W	5VSB	28h (40˚C)	The 3rd boundary temperature: When temperature exceeds this boundary, expected FAN1 value will be loaded from segment 3 register (index ACh). When temperature is under this (boundary – hysteresis), expected FAN1 value will be loaded from segment 4 register (index ADh). This byte is 2's complement value ranging from -128˚C ~ 127˚C.

5.4.105 VT 1 Boundary 4 Temperature Register – Index A9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP1	R/W	5VSB	1Eh (30˚C)	The 4th boundary temperature: When temperature exceeds this boundary, expected FAN1 value will be loaded from segment 4 register (index ADh). When temperature is under this (boundary – hysteresis), expected FAN1 value will be loaded from segment 5 register (index AEh). This byte is a 2's complement value ranging from -128˚C ~ 127˚C.

5.4.106 FAN1 SEGMENT 1 SPEED COUNT Register – Index AAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED1	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section

5.4.107 FAN1 SEGMENT 2 SPEED COUNT Register – Index ABh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED1	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.108 FAN1 SEGMENT 3 SPEED COUNT Register – Index ACh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED1	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.109 FAN1 SEGMENT 4 SPEED COUNT Register – Index ADh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED1	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.110 FAN1 SEGMENT 5 SPEED COUNT Register – Index AEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED1	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.111 FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Reset	Default	Description
7	FAN1_TEMP _SEL_DIG	R/W	5VSB	0	This bit companies with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	FAN1_PWM _FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD1 are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FAN1_PWM_FREQ_SEL_EX, FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: 1MHz/((PWM_CLK_DIV+1)*256) where the frequency range is from 3906Hz to 15Hz with the resolution of 15Hz.
5	FAN1_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_ INTERPOLATION _EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP _HIGH_EN	R/W	5VSB	1	This register controls the FAN1 duty movement when temperature is over the highest boundary. 0: The FAN1 duty will increase every segment with the slope selected by FAN1_UP_RATE (Index 9Bh) register. 1: The FAN1 duty will directly jump to the value of FAN1_SEG1 (Index AAh). This bit only activates in the duty mode.
2	FAN1_JUMP _LOW_EN	R/W	5VSB	1	This register controls the FAN1 duty movement when temperature is under highest (boundary – hysteresis). 0: The FAN1 duty will decrease every segment with the slope selected by FAN1_DN_RATE (Index 9Bh) register. 1: The FAN1 duty will directly jump to the value of FAN1_SEG2 (Index ABh). This bit only activates in the duty mode.
1-0	FAN1_TEMP_SEL	R/W	5VSB	01	This registers company with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 0 (CR70h). 100: fan1 follows IBX/TSI CPU temperature (CR7Ah) 101: fan1 follows IBX PCH temperature (CR7Bh). 110: fan1 follows IBX MCH temperature (CR7Ch). 111: fan1 follows IBX maximum temperature (CR7Dh). Others are reserved.

5.4.112 FAN2 Control Register – Index B0h~BFh

Register 0x[HEX]	Register Name	Default Value MSB							LS B
B0	FAN2 count reading (MSB)	0	0	0	0	1	1	1	1
B1	FAN2 count reading (LSB)	1	1	1	1	1	1	1	1
B2	FAN2 expect speed count value (MSB)	0	0	0	0	0	0	0	0
B3	FAN2 expect speed count value (LSB)	1	0	0	0	0	0	0	0
B4	FAN2 full speed count reading (MSB)	0	0	0	0	0	0	1	1
B5	FAN2 full speed count reading (LSB)	1	1	1	1	1	1	1	1
B6	FAN2 Boundary 1 Temperature Register	0	0	1	1	1	1	0	0
B7	FAN2 Boundary 2 Temperature Register	0	0	1	1	0	0	1	0
B8	FAN2 Boundary 3 Temperature Register	0	0	1	0	1	0	0	0
B9	FAN2 Boundary 4 Temperature Register	0	0	0	1	1	1	1	0
BA	FAN2 Segment 1 Speed Count Register	1	1	1	1	1	1	1	1
BB	FAN2 Segment 2 Speed Count Register	1	1	0	1	1	0	0	1
BC	FAN2 Segment 3 Speed Count Register	1	0	1	1	0	0	1	0
BD	FAN2 Segment 4 Speed Count Register	1	0	0	1	1	0	0	1
BE	FAN2 Segment 5 Speed Count Register	1	0	0	0	0	0	0	0
BF	FAN2 Temperature Mapping Select	0	0	0	1	1	1	1	0

Address	Attribute	Reset	Default Value	Description
B0h	RO	3VCC	8'h0F	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	3VCC	8'hFF	FAN2 count reading (LSB).
B2h	R/W	5VSB	8'h00	RPM mode(CR96 bit2=0): FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. Duty mode (CR96 bit2=1): This byte is reserved byte.
B3h	R/W	5VSB	8'h80	RPM mode(CR96 bit2=0): FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit2=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%

B4h	R/W	5VSB	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	5VSB	8'hFF	FAN2 full speed count reading (LSB).

5.4.113 VT 2 Boundary 1 Temperature Register – Index B6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP2	R/W	5VSB	3Ch (60°C)	The 1st boundary temperature: When temperature exceeds this boundary, expected FAN2 value will be loaded from segment 1 register (index BAh). When temperature is under this (boundary – hysteresis), expected FAN2 value will be loaded from segment 2 register (index BBh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

5.4.114 VT 2 Boundary 2 Temperature Register – Index B7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP2	R/W	5VSB	32 (50°C)	The 2nd boundary temperature: When temperature exceeds this boundary, expected FAN2 value will be loaded from segment 2 register (index BBh). When temperature is under this (boundary – hysteresis), expected FAN2 value will be loaded from segment 3 register (index BCh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

5.4.115 VT 2 Boundary 3 Temperature Register – Index B8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP2	R/W	5VSB	28h (40°C)	The 3rd boundary temperature: When temperature exceeds this boundary, expected FAN2 value will be loaded from segment 3 register (index BCh). When temperature is under this (boundary – hysteresis), expected FAN2 value will be loaded from segment 4 register (index BDh). This byte is a 2's complement value ranging from -128°C ~ 127°C

5.4.116 VT 2 Boundary 4 Temperature Register – Index B9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP2	R/W	5VSB	1Eh (30°C)	The 4th boundary temperature: When temperature exceeds this boundary, expected FAN2 value will be loaded from segment 4 register (index BDh). When temperature is under this (boundary – hysteresis), expected FAN2 value will be loaded from segment 5 register (index BEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

5.4.117 FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED2	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.118 FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED2	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.119 FAN2 SEGMENT 3 SPEED COUNT Register – Index BCh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED2	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.120 FAN2 SEGMENT 4 SPEED COUNT Register – Index BDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED2	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.121 FAN2 SEGMENT 5 SPEED COUNT Register – Index BEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED2	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.122 FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Reset	Default	Description
7	FAN2_TEMP_ SEL_DIG	R/W	5VSB	0	This bit companies with FAN2_TEMP_SEL to select the temperature source for controlling FAN2.
6	FAN2_PWM_ FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD2 are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = {FAN2_PWM_FREQ_SEL_EX, FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: 1MHz/((PWM_CLK_DIV+1)*256) where the frequency range is from 3906Hz to 15Hz with the resolution of 15Hz.
5	FAN2_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_ INTERPOLATION_EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_ HIGH_EN	R/W	5VSB	1	This register controls the FAN2 duty movement when temperature is over the highest boundary. 0: The FAN2 duty will increase every segment with the slope selected by FAN2_UP_RATE (Index 9Bh) register. 1: The FAN2 duty will directly jump to the value of FAN2_SEG1 (Index BAh). This bit only activates in the duty mode.

2	FAN2_JUMP_ LOW_EN	R/W	5VSB	1	This register controls the FAN2 duty movement when temperature is under highest (boundary – hysteresis). 0: The FAN2 duty will decrease every segment with the slope selected by FAN2_DN_RATE (Index 9Bh) register. 1: The FAN2 duty will directly jump to the value of FAN2_SEG2 (Index BBh). This bit only activates in the duty mode.
1-0	FAN2_TEMP_SEL	R/W	5VSB	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR7Eh) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011: fan2 follows temperature 0 (CR70h). 100: fan2 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan2 follows IBEX PCH temperature (CR7Bh). 110: fan2 follows IBEX MCH temperature (CR7Ch). 111: fan2 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

5.4.123 FAN3 Control Register – Index C0h- CFh

Register 0x[HEX]	Register Name	Default Value							
		MSB							LS B
C0	FAN3 count reading (MSB)	0	0	0	0	1	1	1	1
C1	FAN3 count reading (LSB)	1	1	1	1	1	1	1	1
C2	FAN3 expect speed count value (MSB)	0	0	0	0	0	0	0	0
C3	FAN3 expect speed count value (LSB)	1	0	0	0	0	0	0	0
C4	FAN3 full speed count reading (MSB)	0	0	0	0	0	0	1	1
C5	FAN3 full speed count reading (LSB)	1	1	1	1	1	1	1	1
C6	FAN3 Boundary 1 Temperature Register	0	0	1	1	1	1	0	0
C7	FAN3 Boundary 2 Temperature Register	0	0	1	1	0	0	1	0
C8	FAN3 Boundary 3 Temperature Register	0	0	1	0	1	0	0	0
C9	FAN3 Boundary 4 Temperature Register	0	0	0	1	1	1	1	0
CA	FAN3 Segment 1 Speed Count Register	1	1	1	1	1	1	1	1
CB	FAN3 Segment 2 Speed Count Register	1	1	0	1	1	0	0	1
CC	FAN3 Segment 3 Speed Count Register	1	0	1	1	0	0	1	0
CD	FAN3 Segment 4 Speed Count Register	1	0	0	1	1	0	0	1
CE	FAN3 Segment 5 Speed Count Register	1	0	0	0	0	0	0	0
CF	FAN3 Temperature Mapping Select	0	0	0	1	1	1	1	1

Address	Attribute	Reset	Default Value	Description
C0h	RO	3VCC	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	3VCC	8'hFF	FAN3 count reading (LSB).
C2h	R/W	VBAT	8'h00	RPM mode(CR96 bit4=0): FAN3 expect speed count value (MSB), in auto fan mode (CR96 bit5➔0) this register is auto updated by hardware. Duty mode(CR96 bit4=1): This byte is reserved byte.
C3h	R/W	VBAT	8'h80	RPM mode(CR96 bit4=0): FAN3 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit4=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	5VSB	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	5VSB	8'hFF	FAN3 full speed count reading (LSB).

5.4.124 VT 3 Boundary 1 Temperature Register – Index C6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP3	R/W	5VSB	3Ch (60°C)	The 1st boundary temperature: When temperature exceeds this boundary, expected FAN3 value will be loaded from segment 1 register (index CAh). When temperature is under this (boundary – hysteresis), expected FAN3 value will be loaded from segment 2 register (index CBh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

5.4.125 VT 3 Boundary 2 Temperature Register – Index C7h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP3	R/W	5VSB	32 (50°C)	The 2nd boundary temperature: When temperature exceeds this boundary, expected FAN3 value will be loaded from segment 2 register (index CBh). When temperature is under this (boundary – hysteresis), expected FAN3 value will be loaded from segment 3 register (index CCh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

5.4.126 VT 3 Boundary 3 Temperature Register – Index C8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP3	R/W	5VSB	28h (40°C)	The 3rd boundary temperature: When temperature exceeds this boundary, expected FAN3 value will be loaded from segment 32 register (index CCh). When temperature is under this (boundary – hysteresis), expected FAN3 value will be loaded from segment 4 register (index CDh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

5.4.127 VT 3 Boundary 4 Temperature Register – Index C9h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP3	R/W	5VSB	1Eh (30°C)	The 4th boundary temperature: When temperature exceeds this boundary, expected FAN3 value will be loaded from segment 4 register (index CDh). When temperature is under this (boundary – hysteresis), expected FAN3 value will be loaded from segment 5 register (index CDh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

5.4.128 FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED3	R/W	5VSB	FFh (100%)	The meaning of this register is depending on the FAN3_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex:100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.129 FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED3	R/W	5VSB	D9h (85%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.130 FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED3	R/W	5VSB	B2h (70%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.131 FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED3	R/W	5VSB	99h (60%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.132 FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5SPEED3	R/W	5VSB	80h (50%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

5.4.133 FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Reset	Default	Description
7	FAN3_TEMP_ SEL_DIG	R/W	5VSB	0	This bit companies with FAN3_TEMP_SEL select the temperature source for controlling FAN3.

6	FAN3_PWM_ FREQ_SEL	R/W	5VSB	0	This bit and FREQ_SEL_ADD3 are used to select FAN3 PWM frequency. NEW_FREQ_SEL3 = { FAN3_PWM_FREQ_SEL_EX, FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 000: 23.5 KHz 001: 11.75 KHz 010: 5.875 KHz 011: 220 Hz 1xx: 1MHz/((PWM_CLK_DIV+1)*256) where the frequency range is from 3906Hz to 15Hz with the resolution of 15Hz.
5	FAN3_UP_T_EN	R/W	5VSB	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_ INTERPOLATION_EN	R/W	5VSB	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN3_JUMP_ HIGH_EN	R/W	5VSB	1	This register controls the FAN3 duty movement when temperature is over the highest boundary. 0: The FAN3 duty will increase every segment with the slope selected by FAN3_UP_RATE (Index 9Bh) register. 1: The FAN3 duty will directly jump to the value of FAN3_SEG1 (Index CAh). This bit only activates in the duty mode.
2	FAN3_JUMP_ LOW_EN	R/W	5VSB	1	This register controls the FAN3 duty movement when temperature is under the highest (boundary – hysteresis). 0: The FAN3 duty will decrease every segment with the slope selected by FAN3_DN_RATE (Index 9Bh) register. 1: The FAN3 duty will directly jump to the value of FAN3_SEG2 (Index CBh). This bit only activates in duty mode.
1-0	FAN3_TEMP_SEL	R/W	5VSB	11	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 000: fan3 follows PECI temperature (CR7Eh) 001: fan3 follows temperature 1 (CR72h). 010: fan3 follows temperature 2 (CR74h). 011: fan3 follows temperature 0 (CR70h). 100: fan3 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan3 follows IBEX PCH temperature (CR7Bh). 110: fan3 follows IBEX MCH temperature (CR7Ch). 111: fan3 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

5.5 KBC Registers (CR05)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
FE	PS/2 Swap Register	0	0	0	0	0	0	1	1

5.5.1 KBC Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	KBC_EN	R/W	3VCC	1	0: disable KBC. 1: enable KBC. This bit is power-on strap by RTS2# pin.

5.5.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of KBC command port address. The address of data port is command port address + 4

5.5.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

5.5.4 KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELKIRQ	R/W	LRESET#	1h	Select the IRQ channel for keyboard interrupt.

5.5.5 Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELMIRQ	R/W	LRESET#	Ch	Select the IRQ channel for PS/2 mouse interrupt.

5.5.6 PS/2 Swap Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7	AUTO_SWP_EN	R/W	VBAT	0	Set “1” to enable auto swap function.
6	RE_GEN_INT_EN	R/W	VBAT	0	Set “1” to auto re-generate interrupt every 500ms if interrupt is not serviced.
5	Reserved	R/W	VBAT	0	Reserved
4	KB_MO_SWAP	R/W	VBAT	0	Keyboard Mouse Swap. 0: Keyboard/Mouse is not swapped. 1: Keyboard/Mouse is swapped. This bit could be programmed by user.
3-0	Reserved	R/W	VBAT	-	Reserved

5.6 GPIO Registers (CR06)

5.6.1 GPIO General Register

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB LSB							
30	GPIO Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	GPIO0x IRQ Channel Select Register	-	-	-	-	0	0	0	0
71	GPIO1x IRQ Channel Select Register	-	-	-	-	0	0	0	0
72	GPIO5x IRQ Channel Select Register	-	-	-	-	0	0	0	0
73	GPIO8x IRQ Channel Select Register	-	-	-	-	0	0	0	0
7E	GPIO0x/1x/5x/8x IRQ Share Register	-	-	-	-	0	0	0	0
7F	GPIO0x/1x/5x/8x IRQ Mode Register	0	0	0	0	0	0	0	0

5.6.2 GPIO Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	GPIO_EN	R/W	LRESET#	0	0: disable GPIO I/O port. 1: enable GPIO I/O port.

5.6.3 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_H	R/W	LRESET#	0h	The MSB of GPIO I/O port address.

5.6.4 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	0h	The LSB of GPIO base address.

5.6.5 GPIO0x IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGPIOIRQ	R/W	LRESET#	0h	Select the IRQ channel for GPIO0x interrupt.

5.6.6 GPIO1x IRQ Channel Select Register — Index 71h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGP1IRQ	R/W	LRESET#	0h	Select the IRQ channel for GPIO1x interrupt.

5.6.7 GPIO5x IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGP5IRQ	R/W	LRESET#	0h	Select the IRQ channel for GPIO5x interrupt.

5.6.8 GPIO8x IRQ Channel Select Register — Index 73h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGP8IRQ	R/W	LRESET#	0h	Select the IRQ channel for GPIO8x interrupt.

5.6.9 GPIO0x/1x/5x/8x IRQ Sharing Enable Register — Index 7Eh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	GP8_IRQ_SHARE	R/W	LRESET#	0	0: GPIO8x IRQ is not sharing with other devices. 1: GPIO8x IRQ is sharing with other devices.
2	GP5_IRQ_SHARE	R/W	LRESET#	0	0: GPIO5x IRQ is not sharing with other devices. 1: GPIO5x IRQ is sharing with other devices.
1	GP1_IRQ_SHARE	R/W	LRESET#	0	0: GPIO1x IRQ is not sharing with other devices. 1: GPIO1x IRQ is sharing with other devices.
0	GP0_IRQ_SHARE	R/W	LRESET#	0	0: GPIO0x IRQ is not sharing with other devices. 1: GPIO0x IRQ is sharing with other devices.

5.6.10 GPIO0x/1x/5x/8x IRQ Sharing Mode Register — Index 7Fh

Bit	Name	R/W	Reset	Default	Description
7-6	GP8_IRQ_MODE	R/W	LRESET#	0	GPIO8 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge.

					10 : Sharing IRQ active high Level. 11 : Reserved.
5-4	GP5_IRQ_MODE	R/W	LRESET#	0	GPIO5 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge. 10 : Sharing IRQ active high Level. 11 : Reserved.
3-2	GP1_IRQ_MODE	R/W	LRESET#	0	GPIO1 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge. 10 : Sharing IRQ active high Level. 11 : Reserved.
1-0	GP0_IRQ_MODE	R/W	LRESET#	0	GPIO0 IRQ sharing mode: 00 : Sharing IRQ active low Level. 01 : Sharing IRQ active high edge. 10 : Sharing IRQ active high Level. 11 : Reserved.

**This bit is effective when IRQ is sharing with other device (for example: GP8_IRQ_SHARE is "1").*

5.6.11 GPIO0x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB LSB							
F0	GPIO0x Output Enable Register	0	0	0	0	0	0	0	0
F1	GPIO0x Output Data Register	0	0	0	0	1	1	1	1
F2	GPIO0x Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO0x Drive Enable Register	0	0	0	0	0	0	0	0
F4	GPIO0x SMI Enable Register	0	0	0	0	0	0	0	0
F5	GPIO0x SMI Detect Select Register	1	1	1	1	1	1	1	1
F6	GPIO0x SMI Status Register	0	0	0	0	0	0	0	0
F7	GPIO0x Pulse Width Select Register	0	0	0	0	0	0	0	0
F8	GPIO0x Output Mode Register	0	0	0	0	0	0	0	0

5.6.12 GPIO0x Output Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_OE	R/W	5VSB	0	0: GPIO07 is input. 1: GPIO07 is output.
6	GPIO06_OE	R/W	5VSB	0	0: GPIO06 is input. 1: GPIO06 is output.
5	GPIO05_OE	R/W	5VSB	0	0: GPIO05 is input. 1: GPIO05 is output.

4	GPIO04_OE	R/W	5VSB	0	0: GPIO04 is input. 1: GPIO04 is output.
3	GPIO03_OE	R/W	5VSB	0	0: GPIO03 is input. 1: GPIO03 is output.
2	GPIO02_OE	R/W	5VSB	0	0: GPIO02 is input. 1: GPIO02 is output.
1	GPIO01_OE	R/W	5VSB	0	0: GPIO01 is input. 1: GPIO01 is output.
0	GPIO00_OE	R/W	5VSB	0	0: GPIO00 is input. 1: GPIO00 is output.

5.6.13 GPIO0x Output Data Register — Index F1h (This byte could be also written by base address + 6)

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DATA	R/W	5VSB	0	0: GPIO07 outputs 0 when in output mode. 1: GPIO07 outputs 1 when in output mode. In pulse mode, write “1” will generate a pulse and data will auto clear to “0”.
6	GPIO06_DATA	R/W	5VSB	0	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs 1 when in output mode. In pulse mode, write “1” will generate a pulse and data will auto clear to “0”.
5	GPIO05_DATA	R/W	5VSB	0	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode. In pulse mode, write “1” will generate a pulse and data will auto clear to “0”.
4	GPIO04_DATA	R/W	5VSB	0	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode. In pulse mode, write “1” will generate a pulse and data will auto clear to “0”.
3	GPIO03_DATA	R/W	5VSB	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_DATA	R/W	5VSB	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_DATA	R/W	5VSB	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_DATA	R/W	5VSB	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

5.6.14 GPIO0x Pin Status Register — Index F2h (This byte could be also read by base address + 6)

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_ST	R	-	-	The pin status of GPIO07.
6	GPIO06_ST	R	-	-	The pin status of GPIO06.
5	GPIO05_ST	R	-	-	The pin status of GPIO05.
4	GPIO04_ST	R	-	-	The pin status of GPIO04.
3	GPIO03_ST	R	-	-	The pin status of GPIO03.
2	GPIO02_ST	R	-	-	The pin status of GPIO02.
1	GPIO01_ST	R	-	-	The pin status of GPIO01.
0	GPIO00_ST	R	-	-	The pin status of GPIO01.

5.6.15 GPIO0x Drive Enable Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DRV_EN	R/W	5VSB	0	GPIO07 Drive Enable. 0: GPIO07 is open drain. 1: GPIO07 is push pull.
6	GPIO06_DRV_EN	R/W	5VSB	0	GPIO06 Drive Enable. 0: GPIO06 is open drain. 1: GPIO06 is push pull.
5	GPIO05_DRV_EN	R/w	5VSB	0	GPIO05 Drive Enable. 0: GPIO05 is open drain. 1: GPIO05 is push pull.
4	GPIO04_DRV_EN	R/W	5VSB	0	GPIO04 Drive Enable. 0: GPIO04 is open drain. 1: GPIO04 is push pull.
3	GPIO03_DRV_EN	R/W	5VSB	0	GPIO03 Drive Enable. 0: GPIO03 is open drain. 1: GPIO03 is push pull.
2	GPIO02_DRV_EN	R/W	5VSB	0	GPIO02 Drive Enable. 0: GPIO02 is open drain. 1: GPIO02 is push pull.
1	GPIO01_DRV_EN	R/W	5VSB	0	GPIO01 Drive Enable. 0: GPIO01 is open drain. 1: GPIO01 is push pull.
0	GPIO00_DRV_EN	R/W	5VSB	0	GPIO00 Drive Enable. 0: GPIO00 is open drain. 1: GPIO00 is push pull.

5.6.16 GPIO0x SMI Enable Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO07_SMI_ST is set.
6	GPIO06_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO06_SMI_ST is set.
5	GPIO05_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO05_SMI_ST is set.
4	GPIO04_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO04_SMI_ST is set.
3	GPIO03_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO03_SMI_ST is set.
2	GPIO02_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO02_SMI_ST is set.
1	GPIO01_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO01_SMI_ST is set.
0	GPIO00_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO00_SMI_ST is set.

5.6.17 GPIO0x SMI Detect Select Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DET_SEL	R/W	5VSB	1	0: GPIO07 rising edge to set SMI status. 1: GPIO07 falling edge to set SMI status.
6	GPIO06_DET_SEL	R/W	5VSB	1	0: GPIO06 rising edge to set SMI status. 1: GPIO06 falling edge to set SMI status.
5	GPIO05_DET_SEL	R/W	5VSB	1	0: GPIO05 rising edge to set SMI status. 1: GPIO05 falling edge to set SMI status.
4	GPIO04_DET_SEL	R/W	5VSB	1	0: GPIO04 rising edge to set SMI status. 1: GPIO04 falling edge to set SMI status.
3	GPIO03_DET_SEL	R/W	5VSB	1	0: GPIO03 rising edge to set SMI status. 1: GPIO03 falling edge to set SMI status.
2	GPIO02_DET_SEL	R/W	5VSB	1	0: GPIO02 rising edge to set SMI status. 1: GPIO02 falling edge to set SMI status.
1	GPIO01_DET_SEL	R/W	5VSB	1	0: GPIO01 rising edge to set SMI status. 1: GPIO01 falling edge to set SMI status.
0	GPIO00_DET_SEL	R/W	5VSB	1	0: GPIO00 rising edge to set SMI status. 1: GPIO00 falling edge to set SMI status.

5.6.18 GPIO0x SMI Status Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO07 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO06_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO06 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO05_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO05 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO04_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO04 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO03_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO03 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO02_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO02 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO01_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO01 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO00_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO00 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.6.19 GPIO0x Pulse Width Select Register — Index F7h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_PW_SEL	R/WC	5VSB	00b	GPIO07 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
5-4	GPIO06_PW_SEL	R/WC	5VSB	00b	GPIO06 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
3-2	GPIO05_PW_SEL	R/WC	5VSB	00b	GPIO05 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO04_PW_SEL	R/WC	5VSB	00b	GPIO04 pulse width select: 00: 500us. 01: 1ms. 10: 20ms. 11: 100ms.

5.6.20 GPIO0x Output Mode Register — Index F8h

Bit	Name	R/W	Reset	Default	Description
7-6	GPIO07_MODE	R/WC	5VSB	0	00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
5-4	GPIO06_MODE	R/WC	5VSB	0	00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
3-2	GPIO05_MODE	R/WC	5VSB	0	00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.
1-0	GPIO04_MODE	R/WC	5VSB	0	00: Level mode. 01: Inverted level mode. 10: High pulse mode. 11: Low pulse mode.

5.6.21 GPIO1x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
E0	GPIO1x Output Enable Register	0	0	0	0	0	0	0	0
E1	GPIO1x Output Data Register	1	1	1	1	1	1	1	1
E2	GPIO1x Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1x Drive Enable Register	0	0	0	0	0	0	0	0
E4	GPIO1x SMI Enable Register	0	0	0	0	0	0	0	0
E5	GPIO1x SMI Detect Select Register	1	1	1	1	1	1	1	1
E6	GPIO1x SMI Status Register	0	0	0	0	0	0	0	0

5.6.22 GPIO1x Output Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_OE	R/W	5VSB	0	0: GPIO17 is in input mode. 1: GPIO17 is in output mode.
6	GPIO16_OE	R/W	5VSB	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	5VSB	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	5VSB	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	5VSB	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	5VSB	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	5VSB	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	5VSB	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

5.6.23 GPIO1x Output Data Register — Index E1h (This byte could be also written by base address + 7)

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_DATA	R/W	5VSB	1	0: GPIO17 outputs 0 when in output mode. 1: GPIO17 outputs1 when in output mode.
6	GPIO16_DATA	R/W	5VSB	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_DATA	R/W	5VSB	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_DATA	R/W	5VSB	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.

3	GPIO13_DATA	R/W	5VSB	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_DATA	R/W	5VSB	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_DATA	R/W	5VSB	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_DATA	R/W	5VSB	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

5.6.24 GPIO1x Pin Status Register — Index E2h (This byte could be also read by base address + 7)

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_ST	R	-	-	The pin status of GPIO17.
6	GPIO16_ST	R	-	-	The pin status of GPIO16.
5	GPIO15_ST	R	-	-	The pin status of GPIO15.
4	GPIO14_ST	R	-	-	The pin status of GPIO14.
3	GPIO13_ST	R	-	-	The pin status of GPIO13.
2	GPIO12_ST	R	-	-	The pin status of GPIO12.
1	GPIO11_ST	R	-	-	The pin status of GPIO11.
0	GPIO10_ST	R	-	-	The pin status of GPIO10.

5.6.25 GPIO1x Drive Enable Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_DRV_EN	R/W	5VSB	0	0: GPIO17 is open drain in output mode. 1: GPIO17 is push pull in output mode.
6	GPIO16_DRV_EN	R/W	5VSB	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	5VSB	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	5VSB	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	5VSB	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	5VSB	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	VBAT	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode. This bit is powered by VBAT.
0	GPIO10_DRV_EN	R/W	VBAT	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode. This bit is powered by VBAT.

5.6.26 GPIO1x SMI Enable Register — Index E4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO17_SMI_ST is set.
6	GPIO16_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO16_SMI_ST is set.
5	GPIO15_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO15_SMI_ST is set.
4	GPIO14_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO14_SMI_ST is set.
3	GPIO13_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO13_SMI_ST is set.
2	GPIO12_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO12_SMI_ST is set.
1	GPIO11_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO11_SMI_ST is set.
0	GPIO10_SMI_EN	R/W	5VSB	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO10_SMI_ST is set.

5.6.27 GPIO1x SMI Detect Select Register — Index E5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_DET_SEL	R/W	5VSB	1	0: GPIO17 rising edge to set SMI status. 1: GPIO17 falling edge to set SMI status.
6	GPIO16_DET_SEL	R/W	5VSB	1	0: GPIO16 rising edge to set SMI status. 1: GPIO16 falling edge to set SMI status.
5	GPIO15_DET_SEL	R/W	5VSB	1	0: GPIO15 rising edge to set SMI status. 1: GPIO15 falling edge to set SMI status.
4	GPIO14_DET_SEL	R/W	5VSB	1	0: GPIO14 rising edge to set SMI status. 1: GPIO14 falling edge to set SMI status.
3	GPIO13_DET_SEL	R/W	5VSB	1	0: GPIO13 rising edge to set SMI status. 1: GPIO13 falling edge to set SMI status.
2	GPIO12_DET_SEL	R/W	5VSB	1	0: GPIO12 rising edge to set SMI status. 1: GPIO12 falling edge to set SMI status.
1	GPIO11_DET_SEL	R/W	5VSB	1	0: GPIO11 rising edge to set SMI status. 1: GPIO11 falling edge to set SMI status.
0	GPIO10_DET_SEL	R/W	5VSB	1	0: GPIO10 rising edge to set SMI status. 1: GPIO10 falling edge to set SMI status.

5.6.28 GPIO1x SMI Status Register — Index E6h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO17 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO16_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO16 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO15_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO15 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO14_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO14 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO13_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO13 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO12_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO12 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO11_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO11 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO10_SMI_ST	R/WC	5VSB	0	0: No SMI event. 1: A SMI event will set if GPIO10 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.6.29 GPIO2x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
D0	GPIO2x Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2x Output Data Register	1	1	1	1	1	1	1	1
D2	GPIO2x Pin Status Register	-	-	-	-	-	-	-	-

5.6.30 GPIO2x Output Enable Register — Index D0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_OE	R/W	VBAT	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	VBAT	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	VBAT	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	VBAT	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	VBAT	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	VBAT	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	VBAT	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	VBAT	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

5.6.31 GPIO2x Output Data Register — Index D1h (This byte could be also written by base address + 8 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_DATA	R/W	VBAT	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs1 when in output mode.
6	GPIO26_DATA	R/W	VBAT	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs1 when in output mode.
5	GPIO25_DATA	R/W	VBAT	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_DATA	R/W	VBAT	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_DATA	R/W	VBAT	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_DATA	R/W	VBAT	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_DATA	R/W	VBAT	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_DATA	R/W	VBAT	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

5.6.32 GPIO2x Pin Status Register — Index D2h (This byte could be also read by base address + 8 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_ST	R	-	-	The pin status of GPIO27.
6	GPIO26_ST	R	-	-	The pin status of GPIO26.
5	GPIO25_ST	R	-	-	The pin status of GPIO25.
4	GPIO24_ST	R	-	-	The pin status of GPIO24.
3	GPIO23_ST	R	-	-	The pin status of GPIO23.
2	GPIO22_ST	R	-	-	The pin status of GPIO22.
1	GPIO21_ST	R	-	-	The pin status of GPIO21.
0	GPIO20_ST	R	-	-	The pin status of GPIO20.

5.6.33 GPIO3x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
C0	GPIO3x Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3x Output Data Register	1	1	1	1	1	1	1	1
C2	GPIO3x Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3x Drive Enable Register	0	0	0	0	0	0	0	0

5.6.34 GPIO3x Output Enable Register — Index C0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_OE	R/W	5VSB	0	0: GPIO37 is input. 1: GPIO37 is output.
6	GPIO36_OE	R/W	5VSB	0	0: GPIO36 is input. 1: GPIO36 is output.
5	GPIO35_OE	R/W	5VSB	0	0: GPIO35 is input. 1: GPIO35 is output.
4	GPIO34_OE	R/W	5VSB	0	0: GPIO34 is input. 1: GPIO34 is output.
3	GPIO33_OE	R/W	5VSB	0	0: GPIO33 is input. 1: GPIO33 is output.
2	GPIO32_OE	R/W	5VSB	0	0: GPIO32 is input. 1: GPIO32 is output.
1	GPIO31_OE	R/W	5VSB	0	0: GPIO31 is input. 1: GPIO31 is output.
0	GPIO30_OE	R/W	5VSB	0	0: GPIO30 is input. 1: GPIO30 is output.

5.6.35 GPIO3x Output Data Register — Index C1h (This byte could be also written by base address + 9 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DATA	R/W	5VSB	1	0: GPIO37 outputs 0 when in output mode. 1: GPIO37 outputs 1 when in output mode.
6	GPIO36_DATA	R/W	5VSB	1	0: GPIO36 outputs 0 when in output mode. 1: GPIO36 outputs 1 when in output mode.
5	GPIO35_DATA	R/W	5VSB	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_DATA	R/W	5VSB	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_DATA	R/W	5VSB	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_DATA	R/W	5VSB	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_DATA	R/W	5VSB	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_DATA	R/W	5VSB	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

5.6.36 GPIO3x Pin Status Register — Index C2h (This byte could be also read by base address + 9 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_ST	R	-	-	The pin status of GPIO37.
6	GPIO36_ST	R	-	-	The pin status of GPIO36.
5	GPIO35_ST	R	-	-	The pin status of GPIO35.
4	GPIO34_ST	R	-	-	The pin status of GPIO34.
3	GPIO33_ST	R	-	-	The pin status of GPIO33.
2	GPIO32_ST	R	-	-	The pin status of GPIO32.
1	GPIO31_ST	R	-	-	The pin status of GPIO31.
0	GPIO30_ST	R	-	-	The pin status of GPIO30.

5.6.37 GPIO3x Drive Enable Register — Index C3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DRV_EN	R/W	5VSB	0	GPIO37 Drive Enable. 0: GPIO37 is open drain. 1: GPIO37 is push pull.
6	GPIO36_DRV_EN	R/W	5VSB	0	GPIO36 Drive Enable. 0: GPIO36 is open drain. 1: GPIO36 is push pull.

5	GPIO35_DRV_EN	R/w	5VSB	0	GPIO35 Drive Enable. 0: GPIO35 is open drain. 1: GPIO35 is push pull.
4	GPIO34_DRV_EN	R/W	5VSB	0	GPIO34 Drive Enable. 0: GPIO34 is open drain. 1: GPIO34 is push pull.
3	GPIO33_DRV_EN	R/W	5VSB	0	GPIO33 Drive Enable. 0: GPIO33 is open drain. 1: GPIO33 is push pull.
2	GPIO32_DRV_EN	R/W	5VSB	0	GPIO32 Drive Enable. 0: GPIO32 is open drain. 1: GPIO32 is push pull.
1	GPIO31_DRV_EN	R/W	5VSB	0	GPIO31 Drive Enable. 0: GPIO31 is open drain. 1: GPIO31 is push pull.
0	GPIO30_DRV_EN	R/W	5VSB	0	GPIO30 Drive Enable. 0: GPIO30 is open drain. 1: GPIO30 is push pull.

5.6.38 GPIO4x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
B0	GPIO4x Output Enable Register	0	0	0	0	0	0	0	0
B1	GPIO4x Output Data Register	1	1	1	1	1	1	1	1
B2	GPIO4x Pin Status Register	-	-	-	-	-	-	-	-
B3	GPIO4x Driver Enable Register	0	0	0	0	0	0	0	0

5.6.39 GPIO4x Output Enable Register — Index B0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_OE	R/W	5VSB	0	0: GPIO47 is input. 1: GPIO47 is output.
6	GPIO46_OE	R/W	5VSB	0	0: GPIO46 is input. 1: GPIO46 is output.
5	GPIO45_OE	R/W	5VSB	0	0: GPIO45 is input. 1: GPIO45 is output.
4	GPIO44_OE	R/W	5VSB	0	0: GPIO44 is input. 1: GPIO44 is output.
3	GPIO43_OE	R/W	5VSB	0	0: GPIO43 is input. 1: GPIO43 is output.

2	GPIO42_OE	R/W	5VSB	0	0: GPIO42 is input. 1: GPIO42 is output.
1	GPIO41_OE	R/W	5VSB	0	0: GPIO41 is input. 1: GPIO41 is output.
0	GPIO40_OE	R/W	5VSB	0	0: GPIO40 is input. 1: GPIO40 is output.

5.6.40 GPIO4x Output Data Register — Index B1h (This byte could be also written by base address + 10 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DATA	R/W	5VSB	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_DATA	R/W	5VSB	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_DATA	R/W	5VSB	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_DATA	R/W	5VSB	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3	GPIO43_DATA	R/W	5VSB	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs 1 when in output mode.
2	GPIO42_DATA	R/W	5VSB	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs 1 when in output mode.
1	GPIO41_DATA	R/W	5VSB	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs 1 when in output mode.
0	GPIO40_DATA	R/W	5VSB	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs 1 when in output mode.

5.6.41 GPIO4x Pin Status Register — Index B2h (This byte could be also read by base address + 10 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_ST	R	-	-	The pin status of GPIO47.
6	GPIO46_ST	R	-	-	The pin status of GPIO46.
5	GPIO45_ST	R	-	-	The pin status of GPIO45.
4	GPIO44_ST	R	-	-	The pin status of GPIO44.
3	GPIO43_ST	R	-	-	The pin status of GPIO43.
2	GPIO42_ST	R	-	-	The pin status of GPIO42.
1	GPIO41_ST	R	-	-	The pin status of GPIO41.
0	GPIO40_ST	R	-	-	The pin status of GPIO40.

5.6.42 GPIO4x Drive Enable Register — Index B3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DRV_EN	R/W	5VSB	0	GPIO47 Drive Enable. 0: GPIO47 is open drain. 1: GPIO47 is push pull.
6	GPIO46_DRV_EN	R/W	5VSB	0	GPIO46 Drive Enable. 0: GPIO46 is open drain. 1: GPIO46 is push pull.
5	GPIO45_DRV_EN	R/w	5VSB	0	GPIO45 Drive Enable. 0: GPIO45 is open drain. 1: GPIO45 is push pull.
4	GPIO44_DRV_EN	R/W	5VSB	0	GPIO44 Drive Enable. 0: GPIO44 is open drain. 1: GPIO44 is push pull.
3	GPIO43_DRV_EN	R/W	5VSB	0	GPIO43 Drive Enable. 0: GPIO43 is open drain. 1: GPIO43 is push pull.
2	GPIO42_DRV_EN	R/W	5VSB	0	GPIO42 Drive Enable. 0: GPIO42 is open drain. 1: GPIO42 is push pull.
1	GPIO41_DRV_EN	R/W	5VSB	0	GPIO41 Drive Enable. 0: GPIO41 is open drain. 1: GPIO41 is push pull.
0	GPIO40_DRV_EN	R/W	5VSB	0	GPIO40 Drive Enable. 0: GPIO40 is open drain. 1: GPIO40 is push pull.

5.6.43 GPIO5x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
A0	GPIO5x Output Enable Register	0	0	0	0	0	0	0	0
A1	GPIO5x Output Data Register	1	1	1	1	1	1	1	1
A2	GPIO5x Pin Status Register	-	-	-	-	-	-	-	-
A4	GPIO5x SMI Enable Register	0	0	0	0	0	0	0	0
A5	GPIO5x SMI Detect Select Register	1	1	1	1	1	1	1	1
A6	GPIO5x SMI Status Register	0	0	0	0	0	0	0	0

5.6.44 GPIO5x Output Enable Register — Index A0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_OE	R/W	3VCC	0	0: GPIO57 is in input mode. 1: GPIO57 is in output mode.

6	GPIO56_OE	R/W	3VCC	0	0: GPIO56 is in input mode. 1: GPIO56 is in output mode.
5	GPIO55_OE	R/W	3VCC	0	0: GPIO55 is in input mode. 1: GPIO55 is in output mode.
4	GPIO54_OE	R/W	3VCC	0	0: GPIO54 is in input mode. 1: GPIO54 is in output mode.
3	GPIO53_OE	R/W	3VCC	0	0: GPIO53 is in input mode. 1: GPIO53 is in output mode.
2	GPIO52_OE	R/W	3VCC	0	0: GPIO52 is in input mode. 1: GPIO52 is in output mode.
1	GPIO51_OE	R/W	3VCC	0	0: GPIO51 is in input mode. 1: GPIO51 is in output mode.
0	GPIO50_OE	R/W	3VCC	0	0: GPIO50 is in input mode. 1: GPIO50 is in output mode.

5.6.45 GPIO5x Output Data Register — Index A1h (This byte could be also written by base address + 5)

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_DATA	R/W	3VCC	1	0: GPIO57 outputs 0 when in output mode. 1: GPIO57 outputs 1 when in output mode.
6	GPIO56_DATA	R/W	3VCC	1	0: GPIO56 outputs 0 when in output mode. 1: GPIO56 outputs 1 when in output mode.
5	GPIO55_DATA	R/W	3VCC	1	0: GPIO55 outputs 0 when in output mode. 1: GPIO55 outputs 1 when in output mode.
4	GPIO54_DATA	R/W	3VCC	1	0: GPIO54 outputs 0 when in output mode. 1: GPIO54 outputs 1 when in output mode.
3	GPIO53_DATA	R/W	3VCC	1	0: GPIO53 outputs 0 when in output mode. 1: GPIO53 outputs 1 when in output mode.
2	GPIO52_DATA	R/W	3VCC	1	0: GPIO52 outputs 0 when in output mode. 1: GPIO52 outputs 1 when in output mode.
1	GPIO51_DATA	R/W	3VCC	1	0: GPIO51 outputs 0 when in output mode. 1: GPIO51 outputs 1 when in output mode.
0	GPIO50_DATA	R/W	3VCC	1	0: GPIO50 outputs 0 when in output mode. 1: GPIO50 outputs 1 when in output mode.

5.6.46 GPIO5x Pin Status Register — Index A2h (This byte could be also read by base address + 5)

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_ST	R	-	-	The pin status of GPIO57.
6	GPIO56_ST	R	-	-	The pin status of GPIO56.
5	GPIO55_ST	R	-	-	The pin status of GPIO55.
4	GPIO54_ST	R	-	-	The pin status of GPIO54.

3	GPIO53_ST	R	-	-	The pin status of GPIO53.
2	GPIO52_ST	R	-	-	The pin status of GPIO52.
1	GPIO51_ST	R	-	-	The pin status of GPIO51.
0	GPIO50_ST	R	-	-	The pin status of GPIO50.

5.6.47 GPIO5x SMI Enable Register — Index A4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO57_SMI_ST is set.
6	GPIO56_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO56_SMI_ST is set.
5	GPIO55_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO55_SMI_ST is set.
4	GPIO54_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO54_SMI_ST is set.
3	GPIO53_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO53_SMI_ST is set.
2	GPIO52_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO52_SMI_ST is set.
1	GPIO51_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO51_SMI_ST is set.
0	GPIO50_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO50_SMI_ST is set.

5.6.48 GPIO5x SMI Detect Select Register — Index A5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_DET_SEL	R/W	3VCC	1	0: GPIO57 rising edge to set SMI status. 1: GPIO57 falling edge to set SMI status.
6	GPIO56_DET_SEL	R/W	3VCC	1	0: GPIO56 rising edge to set SMI status. 1: GPIO56 falling edge to set SMI status.
5	GPIO55_DET_SEL	R/W	3VCC	1	0: GPIO55 rising edge to set SMI status. 1: GPIO55 falling edge to set SMI status.
4	GPIO54_DET_SEL	R/W	3VCC	1	0: GPIO54 rising edge to set SMI status. 1: GPIO54 falling edge to set SMI status.
3	GPIO53_DET_SEL	R/W	3VCC	1	0: GPIO53 rising edge to set SMI status. 1: GPIO53 falling edge to set SMI status.
2	GPIO52_DET_SEL	R/W	3VCC	1	0: GPIO52 rising edge to set SMI status. 1: GPIO52 falling edge to set SMI status.

1	GPIO51_DET_SEL	R/W	3VCC	1	0: GPIO51 rising edge to set SMI status. 1: GPIO51 falling edge to set SMI status.
0	GPIO50_DET_SEL	R/W	3VCC	1	0: GPIO50 rising edge to set SMI status. 1: GPIO50 falling edge to set SMI status.

5.6.49 GPIO5x SMI Status Register — Index A6h

Bit	Name	R/W	Reset	Default	Description
7	GPIO57_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO57 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO56_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO56 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO55_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO55 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO54_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO54 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO53_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO53 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO52_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO52 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO51_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO51 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO50_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO50 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.6.50 GPIO6x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
90	GPIO6x Output Enable Register	0	0	0	0	0	0	0	0
91	GPIO6x Output Data Register	1	1	1	1	1	1	1	1
92	GPIO6x Pin Status Register	-	-	-	-	-	-	-	-
93	GPIO6x Drive Enable Register	0	0	0	0	0	0	0	0

5.6.51 GPIO6x Output Enable Register — Index 90h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_OE	R/W	3VCC	0	0: GPIO67 is in input mode. 1: GPIO67 is in output mode.
6	GPIO66_OE	R/W	3VCC	0	0: GPIO66 is in input mode. 1: GPIO65 is in output mode.
5	GPIO65_OE	R/W	3VCC	0	0: GPIO65 is in input mode. 1: GPIO65 is in output mode.
4	GPIO64_OE	R/W	3VCC	0	0: GPIO64 is in input mode. 1: GPIO64 is in output mode.
3	GPIO63_OE	R/W	3VCC	0	0: GPIO63 is in input mode. 1: GPIO63 is in output mode.
2	GPIO62_OE	R/W	3VCC	0	0: GPIO62 is in input mode. 1: GPIO62 is in output mode.
1	GPIO61_OE	R/W	3VCC	0	0: GPIO61 is in input mode. 1: GPIO61 is in output mode.
0	GPIO60_OE	R/W	3VCC	0	0: GPIO60 is in input mode. 1: GPIO60 is in output mode.

5.6.52 GPIO6x Output Data Register — Index 91h (This byte could be also written by base address + 4)

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_DATA	R/W	3VCC	1	0: GPIO67 outputs 0 when in output mode. 1: GPIO67 outputs 1 when in output mode.
6	GPIO66_DATA	R/W	3VCC	1	0: GPIO66 outputs 0 when in output mode. 1: GPIO66 outputs 1 when in output mode.
5	GPIO65_DATA	R/W	3VCC	1	0: GPIO65 outputs 0 when in output mode. 1: GPIO65 outputs 1 when in output mode.
4	GPIO64_DATA	R/W	3VCC	1	0: GPIO64 outputs 0 when in output mode. 1: GPIO64 outputs 1 when in output mode.
3	GPIO63_DATA	R/W	3VCC	1	0: GPIO63 outputs 0 when in output mode. 1: GPIO63 outputs 1 when in output mode.

2	GPIO62_DATA	R/W	3VCC	1	0: GPIO62 outputs 0 when in output mode. 1: GPIO62 outputs 1 when in output mode.
1	GPIO61_DATA	R/W	3VCC	1	0: GPIO61 outputs 0 when in output mode. 1: GPIO61 outputs 1 when in output mode.
0	GPIO60_DATA	R/W	3VCC	1	0: GPIO60 outputs 0 when in output mode. 1: GPIO60 outputs 1 when in output mode.

5.6.53 GPIO6x Pin Status Register — Index 92h (This byte could be also read by base address + 4)

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_ST	R	-	-	The pin status of GPIO67.
6	GPIO66_ST	R	-	-	The pin status of GPIO66.
5	GPIO65_ST	R	-	-	The pin status of GPIO65.
4	GPIO64_ST	R	-	-	The pin status of GPIO64.
3	GPIO63_ST	R	-	-	The pin status of GPIO63.
2	GPIO62_ST	R	-	-	The pin status of GPIO62.
1	GPIO61_ST	R	-	-	The pin status of GPIO61.
0	GPIO60_ST	R	-	-	The pin status of GPIO60.

5.6.54 GPIO6x Drive Enable Register — Index 93h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_DRV_EN	R/W	3VCC	0	0: GPIO67 is open drain in output mode. 1: Reserved.
6	GPIO66_DRV_EN	R/W	3VCC	0	0: GPIO66 is open drain in output mode. 1: GPIO66 is push pull in output mode.
5	GPIO65_DRV_EN	R/W	3VCC	0	0: GPIO65 is open drain in output mode. 1: GPIO65 is push pull in output mode.
4	GPIO64_DRV_EN	R/W	3VCC	0	0: GPIO64 is open drain in output mode. 1: GPIO64 is push pull in output mode.
3	GPIO63_DRV_EN	R/W	3VCC	0	0: GPIO63 is open drain in output mode. 1: GPIO63 is push pull in output mode.
2	GPIO62_DRV_EN	R/W	3VCC	0	0: GPIO62 is open drain in output mode. 1: GPIO62 is push pull in output mode.
1	GPIO61_DRV_EN	R/W	3VCC	0	0: GPIO61 is open drain in output mode. 1: GPIO61 is push pull in output mode.
0	GPIO60_DRV_EN	R/W	3VCC	0	0: GPIO60 is open drain in output mode. 1: GPIO60 is push pull in output mode.

5.6.55 GPIO7x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
80	GPIO7x Output Enable Register	0	0	0	0	0	0	0	0
81	GPIO7x Output Data Register	1	1	1	1	1	1	1	1
82	GPIO7x Pin Status Register	-	-	-	-	-	-	-	-
83	GPIO7x Drive Enable Register	0	0	0	0	0	0	0	0

5.6.56 GPIO7x Output Enable Register — Index 80h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_OE	R/W	3VCC	0	0: GPIO77 is in input mode. 1: GPIO77 is in output mode.
6	GPIO76_OE	R/W	3VCC	0	0: GPIO76 is in input mode. 1: GPIO75 is in output mode.
5	GPIO75_OE	R/W	3VCC	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.
4	GPIO74_OE	R/W	3VCC	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	3VCC	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.
2	GPIO72_OE	R/W	3VCC	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.
1	GPIO71_OE	R/W	3VCC	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	3VCC	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

5.6.57 GPIO7x Output Data Register — Index 81h (This byte could be also written by base address + 3)

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_DATA	R/W	3VCC	1	0: GPIO77 outputs 0 when in output mode. 1: GPIO77 outputs 1 when in output mode.
6	GPIO76_DATA	R/W	3VCC	1	0: GPIO76 outputs 0 when in output mode. 1: GPIO76 outputs 1 when in output mode.
5	GPIO75_DATA	R/W	3VCC	1	0: GPIO75 outputs 0 when in output mode. 1: GPIO75 outputs 1 when in output mode.
4	GPIO74_DATA	R/W	3VCC	1	0: GPIO74 outputs 0 when in output mode. 1: GPIO74 outputs 1 when in output mode.
3	GPIO73_DATA	R/W	3VCC	1	0: GPIO73 outputs 0 when in output mode. 1: GPIO73 outputs 1 when in output mode.
2	GPIO72_DATA	R/W	3VCC	1	0: GPIO72 outputs 0 when in output mode. 1: GPIO72 outputs 1 when in output mode.

1	GPIO71_DATA	R/W	3VCC	1	0: GPIO71 outputs 0 when in output mode. 1: GPIO71 outputs 1 when in output mode.
0	GPIO70_DATA	R/W	3VCC	1	0: GPIO70 outputs 0 when in output mode. 1: GPIO70 outputs 1 when in output mode.

5.6.58 GPIO7x Pin Status Register — Index 82h (This byte could be also read by base address + 3)

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_ST	R	-	-	The pin status of GPIO77.
6	GPIO76_ST	R	-	-	The pin status of GPIO76.
5	GPIO75_ST	R	-	-	The pin status of GPIO75.
4	GPIO74_ST	R	-	-	The pin status of GPIO74.
3	GPIO73_ST	R	-	-	The pin status of GPIO73.
2	GPIO72_ST	R	-	-	The pin status of GPIO72.
1	GPIO71_ST	R	-	-	The pin status of GPIO71.
0	GPIO70_ST	R	-	-	The pin status of GPIO70.

5.6.59 GPIO7x Drive Enable Register — Index 83h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_DRV_EN	R/W	3VCC	0	0: GPIO77 is open drain in output mode. 1: GPIO77 is push pull in output mode.
6	GPIO76_DRV_EN	R/W	3VCC	0	0: GPIO76 is open drain in output mode. 1: GPIO76 is push pull in output mode.
5	GPIO75_DRV_EN	R/W	3VCC	0	0: GPIO75 is open drain in output mode. 1: GPIO75 is push pull in output mode.
4	GPIO74_DRV_EN	R/W	3VCC	0	0: GPIO74 is open drain in output mode. 1: GPIO74 is push pull in output mode.
3	GPIO73_DRV_EN	R/W	3VCC	0	0: GPIO73 is open drain in output mode. 1: GPIO73 is push pull in output mode.
2	GPIO72_DRV_EN	R/W	3VCC	0	0: GPIO72 is open drain in output mode. 1: GPIO72 is push pull in output mode.
1	GPIO71_DRV_EN	R/W	3VCC	0	0: GPIO71 is open drain in output mode. 1: GPIO71 is push pull in output mode.
0	GPIO70_DRV_EN	R/W	3VCC	0	0: GPIO70 is open drain in output mode. 1: GPIO70 is push pull in output mode.

5.6.60 GPIO8x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
88	GPIO8x Output Enable Register	0	0	0	0	0	0	0	0
89	GPIO8x Output Data Register	1	1	1	1	1	1	1	1
8A	GPIO8x Pin Status Register	-	-	-	-	-	-	-	-
8B	GPIO8x Drive Enable Register	0	0	0	0	0	0	0	0
8C	GPIO8x SMI Enable Register	0	0	0	0	0	0	0	0
8D	GPIO8x SMI Detect Select Register	1	1	1	1	1	1	1	1
8E	GPIO8x SMI Status Register	0	0	0	0	0	0	0	0

5.6.61 GPIO8x Output Enable Register — Index 88h

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_OE	R/W	3VCC	0	0: GPIO87 is in input mode. 1: GPIO87 is in output mode.
6	GPIO86_OE	R/W	3VCC	0	0: GPIO86 is in input mode. 1: GPIO85 is in output mode.
5	GPIO85_OE	R/W	3VCC	0	0: GPIO85 is in input mode. 1: GPIO85 is in output mode.
4	GPIO84_OE	R/W	3VCC	0	0: GPIO84 is in input mode. 1: GPIO84 is in output mode.
3	GPIO83_OE	R/W	3VCC	0	0: GPIO83 is in input mode. 1: GPIO83 is in output mode.
2	GPIO82_OE	R/W	3VCC	0	0: GPIO82 is in input mode. 1: GPIO82 is in output mode.
1	GPIO81_OE	R/W	3VCC	0	0: GPIO81 is in input mode. 1: GPIO81 is in output mode.
0	GPIO80_OE	R/W	3VCC	0	0: GPIO80 is in input mode. 1: GPIO80 is in output mode.

5.6.62 GPIO8x Output Data Register — Index 89h (This byte could be also written by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_DATA	R/W	3VCC	1	0: GPIO87 outputs 0 when in output mode. 1: GPIO87 outputs 1 when in output mode.
6	GPIO86_DATA	R/W	3VCC	1	0: GPIO86 outputs 0 when in output mode. 1: GPIO86 outputs 1 when in output mode.
5	GPIO85_DATA	R/W	3VCC	1	0: GPIO85 outputs 0 when in output mode. 1: GPIO85 outputs 1 when in output mode.
4	GPIO84_DATA	R/W	3VCC	1	0: GPIO84 outputs 0 when in output mode. 1: GPIO84 outputs 1 when in output mode.

3	GPIO83_DATA	R/W	3VCC	1	0: GPIO83 outputs 0 when in output mode. 1: GPIO83 outputs 1 when in output mode.
2	GPIO82_DATA	R/W	3VCC	1	0: GPIO82 outputs 0 when in output mode. 1: GPIO82 outputs 1 when in output mode.
1	GPIO81_DATA	R/W	3VCC	1	0: GPIO81 outputs 0 when in output mode. 1: GPIO81 outputs 1 when in output mode.
0	GPIO80_DATA	R/W	3VCC	1	0: GPIO80 outputs 0 when in output mode. 1: GPIO80 outputs 1 when in output mode.

5.6.63 GPIO8x Pin Status Register — Index 8Ah (This byte could be also read by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_ST	R	-	-	The pin status of GPIO87.
6	GPIO86_ST	R	-	-	The pin status of GPIO86.
5	GPIO85_ST	R	-	-	The pin status of GPIO85.
4	GPIO84_ST	R	-	-	The pin status of GPIO84.
3	GPIO83_ST	R	-	-	The pin status of GPIO83.
2	GPIO82_ST	R	-	-	The pin status of GPIO82.
1	GPIO81_ST	R	-	-	The pin status of GPIO81.
0	GPIO80_ST	R	-	-	The pin status of GPIO80.

5.6.64 GPIO8x Drive Enable Register — Index 8Bh

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_DRV_EN	R/W	3VCC	0	0: GPIO87 is open drain in output mode. 1: GPIO87 is push pull in output mode.
6	GPIO86_DRV_EN	R/W	3VCC	0	0: GPIO86 is open drain in output mode. 1: GPIO86 is push pull in output mode.
5	GPIO85_DRV_EN	R/W	3VCC	0	0: GPIO85 is open drain in output mode. 1: GPIO85 is push pull in output mode.
4	GPIO84_DRV_EN	R/W	3VCC	0	0: GPIO84 is open drain in output mode. 1: GPIO84 is push pull in output mode.
3	GPIO83_DRV_EN	R/W	3VCC	0	0: GPIO83 is open drain in output mode. 1: GPIO83 is push pull in output mode.
2	GPIO82_DRV_EN	R/W	3VCC	0	0: GPIO82 is open drain in output mode. 1: GPIO82 is push pull in output mode.
1	GPIO81_DRV_EN	R/W	3VCC	0	0: GPIO81 is open drain in output mode. 1: GPIO81 is push pull in output mode.
0	GPIO80_DRV_EN	R/W	3VCC	0	0: GPIO80 is open drain in output mode. 1: GPIO80 is push pull in output mode.

5.6.65 GPIO8x SMI Enable Register — Index 8Ch

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO87_SMI_ST is set.
6	GPIO86_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO86_SMI_ST is set.
5	GPIO85_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO85_SMI_ST is set.
4	GPIO84_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO84_SMI_ST is set.
3	GPIO83_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO83_SMI_ST is set.
2	GPIO82_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO82_SMI_ST is set.
1	GPIO81_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO81_SMI_ST is set.
0	GPIO80_SMI_EN	R/W	3VCC	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO80_SMI_ST is set.

5.6.66 GPIO8x SMI Detect Select Register — Index 8Dh

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_DET_SEL	R/W	3VCC	1	0: GPIO87 rising edge to set SMI status. 1: GPIO87 falling edge to set SMI status.
6	GPIO86_DET_SEL	R/W	3VCC	1	0: GPIO86 rising edge to set SMI status. 1: GPIO86 falling edge to set SMI status.
5	GPIO85_DET_SEL	R/W	3VCC	1	0: GPIO85 rising edge to set SMI status. 1: GPIO85 falling edge to set SMI status.
4	GPIO84_DET_SEL	R/W	3VCC	1	0: GPIO84 rising edge to set SMI status. 1: GPIO84 falling edge to set SMI status.
3	GPIO83_DET_SEL	R/W	3VCC	1	0: GPIO83 rising edge to set SMI status. 1: GPIO83 falling edge to set SMI status.
2	GPIO82_DET_SEL	R/W	3VCC	1	0: GPIO82 rising edge to set SMI status. 1: GPIO82 falling edge to set SMI status.
1	GPIO81_DET_SEL	R/W	3VCC	1	0: GPIO81 rising edge to set SMI status. 1: GPIO81 falling edge to set SMI status.
0	GPIO80_DET_SEL	R/W	3VCC	1	0: GPIO80 rising edge to set SMI status. 1: GPIO80 falling edge to set SMI status.

5.6.67 GPIO8x SMI Status Register — Index 8Eh

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO87 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO86_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO86 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO85_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO85 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO84_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO84 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO83_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO83 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO82_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO82 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO81_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO81 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO80_SMI_ST	R/WC	3VCC	0	0: No SMI event. 1: A SMI event will set if GPIO80 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.6.68 GPIO9x Configuration Registers

Register 0x[HEX]	Register Name	Default Value MSB							LSB
98	GPIO9x Output Enable Register	0	0	0	0	0	0	0	0
99	GPIO9x Output Data Register	1	1	1	1	1	1	1	1
9A	GPIO9x Pin Status Register	-	-	-	-	-	-	-	-
9B	GPIO9x Drive Enable Register	0	0	0	0	0	0	0	0

5.6.69 GPIO9x Output Enable Register — Index 98h

Bit	Name	R/W	Reset	Default	Description
7	GPIO97_OE	R/W	3VCC	0	0: GPIO97 is in input mode. 1: GPIO96 is in output mode.
6	GPIO96_OE	R/W	3VCC	0	0: GPIO96 is in input mode. 1: GPIO96 is in output mode.
5	GPIO95_OE	R/W	3VCC	0	0: GPIO95 is in input mode. 1: GPIO95 is in output mode.
4	GPIO94_OE	R/W	3VCC	0	0: GPIO94 is in input mode. 1: GPIO94 is in output mode.
3	GPIO93_OE	R/W	3VCC	0	0: GPIO93 is in input mode. 1: GPIO93 is in output mode.
2	GPIO92_OE	R/W	3VCC	0	0: GPIO92 is in input mode. 1: GPIO92 is in output mode.
1	GPIO91_OE	R/W	3VCC	0	0: GPIO91 is in input mode. 1: GPIO91 is in output mode.
0	GPIO90_OE	R/W	3VCC	0	0: GPIO90 is in input mode. 1: GPIO90 is in output mode.

5.6.70 GPIO9x Output Data Register — Index 99h (This byte could be also written by base address + 11 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO97_DATA	R/W	3VCC	1	0: GPIO97 outputs 0 when in output mode. 1: GPIO97 outputs 1 when in output mode.
6	GPIO96_DATA	R/W	3VCC	1	0: GPIO96 outputs 0 when in output mode. 1: GPIO96 outputs 1 when in output mode.
5	GPIO95_DATA	R/W	3VCC	1	0: GPIO95 outputs 0 when in output mode. 1: GPIO95 outputs 1 when in output mode.
4	GPIO94_DATA	R/W	3VCC	1	0: GPIO94 outputs 0 when in output mode. 1: GPIO94 outputs 1 when in output mode.
3	GPIO93_DATA	R/W	3VCC	1	0: GPIO93 outputs 0 when in output mode. 1: GPIO93 outputs 1 when in output mode.
2	GPIO92_DATA	R/W	3VCC	1	0: GPIO92 outputs 0 when in output mode. 1: GPIO92 outputs 1 when in output mode.
1	GPIO91_DATA	R/W	3VCC	1	0: GPIO91 outputs 0 when in output mode. 1: GPIO91 outputs 1 when in output mode.
0	GPIO90_DATA	R/W	3VCC	1	0: GPIO90 outputs 0 when in output mode. 1: GPIO90 outputs 1 when in output mode.

5.6.71 GPIO9x Pin Status Register — Index 9Ah (This byte could be also written by base address + 11 if GPIO_DEC_RANGE is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO97_ST	R	-	-	The pin status of GPIO97.
6	GPIO96_ST	R	-	-	The pin status of GPIO96.
5	GPIO95_ST	R	-	-	The pin status of GPIO95.
4	GPIO94_ST	R	-	-	The pin status of GPIO94.
3	GPIO93_ST	R	-	-	The pin status of GPIO93.
2	GPIO92_ST	R	-	-	The pin status of GPIO92.
1	GPIO91_ST	R	-	-	The pin status of GPIO91.
0	GPIO90_ST	R	-	-	The pin status of GPIO90.

5.6.72 GPIO9x Drive Enable Register — Index 9Bh

Bit	Name	R/W	Reset	Default	Description
7	GPIO97_DRV_EN	R/W	3VCC	0	0: GPIO97 is open drain in output mode. 1: GPIO97 is push pull in output mode.
6	GPIO96_DRV_EN	R/W	3VCC	0	0: GPIO96 is open drain in output mode. 1: GPIO96 is push pull in output mode.
5	GPIO95_DRV_EN	R/W	3VCC	0	0: GPIO95 is open drain in output mode. 1: GPIO95 is push pull in output mode.
4	GPIO94_DRV_EN	R/W	3VCC	0	0: GPIO94 is open drain in output mode. 1: GPIO94 is push pull in output mode.
3	GPIO93_DRV_EN	R/W	3VCC	0	0: GPIO93 is open drain in output mode. 1: GPIO93 is push pull in output mode.
2	GPIO92_DRV_EN	R/W	3VCC	0	0: GPIO92 is open drain in output mode. 1: GPIO92 is push pull in output mode.
1	GPIO91_DRV_EN	R/W	3VCC	0	0: GPIO91 is open drain in output mode. 1: GPIO91 is push pull in output mode.
0	GPIO90_DRV_EN	R/W	3VCC	0	0: GPIO90 is open drain in output mode. 1: GPIO90 is push pull in output mode.

5.7 WDT Device Configuration Registers (LDN CR07)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	WDT Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F0	WDT Output Enable Register	0	-	-	-	-	-	-	-
F5	WDT Control Register	0	0	0	0	0	0	0	0
F6	WDT Timer Register	0	0	0	0	0	0	0	0
FA	WDT PME Enable Register	-	0	0	-	-	-	-	0

5.7.1 WDT Device Base Address Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	WDT_EN	R/W	LRESET#	0	0: disable WDT base address. 1: enable WDT base address.

5.7.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of WDT base address.

5.7.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	The LSB of WDT base address.

5.7.4 WDT Control Configuration Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	--		--	Reserved.
6	WDTMOUT_STS	R/W	5VSB	0	If watchdog timeout event is occurred, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	5VSB	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	5VSB	0	Select output mode (0: level, 1: pulse) of WDTRST# by setting this bit.

3	WD_UNIT	R/W	5VSB	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	5VSB	0	Select output polarity of WDTRST# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	5VSB	00b	Select output pulse width of WDTRST# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

5.7.5 WDT Timer Configuration Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME	R/W	3VCC	0h	Time of watchdog timer (0~255)

5.7.6 WDT PME Enable Configuration Register — Index 0Ah

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME	R	5VSB	-	The PME Status. This bit will be set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	5VSB	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5	Reserved	-		-	Reserved
4	WDT_CLK_SEL	R/W	5VSB	1	WDT Clock Source Select 0: Internal Clock. (No CLKIN is needed) 1: External clock derived by CLKIN. (more accurate)
3-1	Reserved	-		-	Reserved
0	WDOUT_EN	R/W	VBAT	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.

5.8 PME, ACPI and ERP Device Configuration Registers (LDN CR0A)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0
E0	ERP Enable Register	0	0	0	0	0	0	0	0
E1	ERP Control Register 1	-	-	0	0	1	1	0	0
E2	ERP Control Register 2	1	0	0	0	1	1	0	0
E3	ERP PSIN De-bounce Register	0	0	0	1	0	0	1	1
E4	ERP RSMRST De-bounce Register	0	0	0	0	1	0	0	1
E5	ERP PWSOUT De-bounce Register	1	1	0	0	0	1	1	1
E6	ERP PS_ON De-bounce Register	0	0	0	0	1	0	0	1
E7	ERP Deep S5 Delay Register	0	1	1	0	0	0	1	1
E8	ERP Wakeup Enable Register	0	0	0	0	0	0	0	0
E9	ERP Deep S3 Delay Register	0	0	0	0	1	1	1	1
EC	ERP Mode Select Register	0	0	0	1	0	1	0	0
ED	ERP WDT Control Register	-	-	-	-	-	-	0	0
EE	ERP WDT Timer	0	0	0	0	0	0	0	0
F0	PME Event Enable 1 Register	0	0	0	0	0	0	0	-
F1	PME Event Status 1 Register	-	-	-	-	-	-	-	-
F2	PME Event Enable 2 Register	0	0	0	0	0	0	0	0
F3	PME Event Status 2 Register	-	-	-	-	-	-	-	-
F4	ACPI Control Register 1	0	0	0	0	0	1	1	1
F5	ACPI Control Register 2	0	0	0	1	1	1	-	-
F6	ACPI Control Register 3	0	0	0	0	0	0	0	0
F8	LED VCC Control Register	0	0	0	0	0	0	0	0
F9	LED VSB Control Register	0	0	0	0	0	0	0	0
FA	LED Additional Control Register	0	0	0	0	0	0	0	0
FB	GPIO PME Enable Register	-	-	-	-	0	0	0	0
FC	DSW Delay Register	-	-	0	0	0	1	1	1
FD	ACPI Control Register 4	0	0	0	0	0	0	0	0
FE	RI De-bounce Register	-	-	-	-	-	-	0	0

5.8.1 PME Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	PME_EN	R/W	5VSB	0	PME global enable register. 0: disable PME. 1: enable PME.

5.8.2 ERP Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	ERP_EN	R/W	VBAT	0	0 : disable ERP function 1: enable ERP function
6	S3_BACK	R/W	VBAT	0	This bit will be set “1” when the system is back from S3 state.
5-2	Reserved	R/W	VBAT	0	Reserved
1	ERP_PME_EN	R/W	VBAT	0	PME event enable. 0: disable PME event. 1: enable PME event, when wakeup event is detected.
0	ERP_PWSOUT_EN	R/W	VBAT	0	PWSOUT# event enable. This bit has no function when ERP_PME_EN is set. 0: disable PWSOUT# event. 1: enable PWSOUT# event, when wakeup event is detected.

5.8.3 ERP Control Register 1 — Index E1h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved
5	S3_ ERP_CTRL1#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL1# will output Low when S3 state. Else If set to “1” ERP_CTRL1# will output High when S3 state.
4	S3 _ ERP_CTRL0#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL0# will output Low when S3 state. Else If set to “1” ERP_CTRL0# will output High when S3 state.
3	S5 _ ERP_CTRL1#_DIS	R/W	VBAT	1	If clear to “0” ERP_CTRL1# will output Low when S5 state. Else If set to “1” ERP_CTRL1# will output High when S5 state.
2	S5 _ ERP_CTRL0#_DIS	R/W	VBAT	1	If clear to “0” ERP_CTRL0# will output Low when S5 state. Else If set to “1” ERP_CTRL0# will output High when S5 state.
1	AC_ ERP_CTRL1#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL1# will output Low when after AC lost. Else If set to “1” ERP_CTRL1# will output High when after AC lost.
0	AC_ ERP_CTRL0#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL0# will output Low when after AC lost. Else If set to “1” ERP_CTRL0# will output High when after AC lost.

5.8.4 ERP Control Register 2 — Index E2h

Bit	Name	R/W	Reset	Default	Description
7	AC_LOST	R	5VSB	1	This bit is AC lost status and writes 1 to this bit will clear it.
6	Reserved	R/W	VBAT	0	Reserved
5	ERP_CTRL_EN[1]	R/W	VBAT	0	0: Disable ERP_CTRL1# assert RSMRST low 1: Enable ERP_CTRL1# assert RSMRST low
4	ERP_CTRL_EN[0]	R/W	VBAT	0	0: Disable ERP_CTRL0# assert RSMRST low 1: Enable ERP_CTRL0# assert RSMRST low
3-2	Reserved	R/W	VBAT	1	Reserved

1	RSMRST_DET_5V_N	R/W	VBAT	0	Device detects 5VSB power ok (4.4V) and VSB3V_IN become high, and after ~50ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check 5VSB power ok.
0	Reserved	R	VBAT	0	Dummy register.

5.8.5 ERP PSIN De-bounce Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7-0	PSIN_DEB_TIME	R/W	VBAT	13h	PSIN# pin input de-bounce time. The unit is 1ms, default is 20ms.

5.8.6 ERP RSMRST De-bounce Register — Index E4h

Bit	Name	R/W	Reset	Default	Description
7-0	RSMRST_DEB_TIME	R/W	VBAT	9h	RSMRST internal de-bounce time. The unit is 1ms and default is 10ms.

5.8.7 ERP PWSOUT Pulse Width Register — Index E5h

Bit	Name	R/W	Reset	Default	Description
7-0	PWSOUT_PW	R/W	VBAT	C7h	PWSOUT output pulse width. The unit is 1ms and default is 200ms.

5.8.8 ERP PS_ON De-bounce Register — Index E6h

Bit	Name	R/W	Reset	Default	Description
7-0	PSON_DEB_TIME	R/W	VBAT	09h	PS_ON# pin input de-bounce time. The unit is 1ms, default is 10ms.

5.8.9 ERP Deep S5 Delay Register — Index E7h

Bit	Name	R/W	Reset	Default	Description
7-0	DS5_DELAY_TIME	R/W	VBAT	63h	The delay time from S5 state to deep S5 state. The unit is 64ms and default is 6.4 sec. Set “0” to disable Deep S5 delay state.

5.8.10 ERP Wakeup Enable Register — Index E8h

Bit	Name	R/W	Reset	Default	Description
7	RI2_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable RI2#, PME# event to wakeup system.

6	Reserved	R/W	VBAT	0	Dummy register.
5	RI1_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable RI1#, PME# event to wakeup system.
4	RING_WAKEUP_EN	R/W	VBAT	1	Set this bit to enable EVENT_IN# event to wakeup system.
3	GP_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable GPIO event to wakeup system.
2	TMOUT_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Timeout event to wakeup system.
1	MO_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Mouse event to wakeup system.
0	KB_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Keyboard event to wakeup system.

5.8.11 ERP Deep S3 Delay Register — Index E9h

Bit	Name	R/W	Reset	Default	Description
7-0	DS3_DELAY_TIME	R/W	VBAT	Fh	The delay time from S3 state to deep S3 state. The unit is 64ms and default is 1.024 sec. Set “0” to disable Deep S3 delay state.

5.8.12 ERP Mode Select Register — Index ECh

Bit	Name	R/W	Reset	Default	Description
7-6	ERP_MODE	R/W	VBAT	0	00: Fintek G3’ mode. 01: Intel DSW + Fintek G3` mode. 10: Reserved. 11: Intel DSW mode.
5	DPWROK_CTRL_EN	R/W	VBAT	0	Set “1” to enable DPWROK reset by ERP_CTRL1#.
4	SOFT_START_EN	R/W	VBAT	1	0: disable ERP soft start. 1: enable ERP soft start.
3-2	SOFT_START_RATE	R/W	VBAT	1h	The soft start rate for ERP_CTRL# turn off to fully turn-on. 00: 25.6ms 01: 51.2ms. 10: 128ms. 11: 256ms.
1-0	Reserved	-	-	-	Reserved

5.8.13 ERP WDT Control Register — Index EDh

Bit	Name	R/W	Reset	Default	Description
7-6	ERP_WD_TIME [11:10]	R/W	VBAT	-	Bit 11 and 10 of WDT_TIME
5	Reserved	R	-	-	Reserved.
4	ERP_WDTMOUT_ STATUS	R	VBAT	-	ERP watchdog timer timeout status. Write 1 to clear.
3-2	ERP_WD_TIME [9:8]	R/W	VBAT	-	Bit 9 and 8 of WDT_TIME

1	WD_UNIT	R/W	VBAT	0	0: unit of WD_TIME is 1 sec. 1: unit of WD_TIME is 1 minute.
0	WD_EN	R/W	VBAT	0	Enable ERP watchdog timer.

5.8.14 ERP WDT Time Register — Index EEh

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME[7:0]	R/W	VBAT	0	ERP watchdog timer count time register. Start to count down when WD_EN is set. When reaching 0, WD_EN will auto clear and WD_TMOUT is set. A wakeup event will assert if enabled

5.8.15 PME Event Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	WDT_PME_EN	R/W	5VSB	0	WDT PME event enable. 0: disable WDT PME event. 1: enable WDT PME event.
5	GP_PME_EN	R/W	5VSB	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.
4	MO_PME_EN	R/W	5VSB	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
3	KB_PME_EN	R/W	5VSB	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
2	HM_PME_EN	R/W	5VSB	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
1	PRT_PME_EN	R/W	5VSB	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
0	Reserved	-	-	-	Reserved.

5.8.16 PME Event Status 1 Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7	ERP_PME_ST	R/WC	5VSB	-	ERP PME event status. 0: ERP has no PME event. 1: ERP has a PME event to assert. Write 1 to clear to be ready for next PME event.

6	WDT_PME_ST	R/WC	5VSB	-	WDT PME event status. 0: WDT has no PME event. 1: WDT has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	GP_PME_ST	R/WC	5VSB	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	MO_PME_ST	R/WC	5VSB	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	KB_PME_ST	R/WC	5VSB	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	HM_PME_ST	R/WC	5VSB	-	Hardware monitors PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	PRT_PME_ST	R/WC	5VSB	-	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	Reserved	-	-	-	Reserved.

5.8.17 PME Event Enable 2 Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7	RI2_PME_EN	R/W	5VSB	0	RI2# PME event enable. 0: disable RI2# PME event. 1: enable RI2# PME event.
6	RI1_PME_EN	R/W	5VSB	0	RI1# PME event enable. 0: disable RI1# PME event. 1: enable RI1# PME event.
5	UR6_PME_EN	R/W	5VSB	0	UART6 PME event enable. 0: disable UART6 PME event. 1: enable UART6 PME event.
4	UR5_PME_EN	R/W	5VSB	0	UART5 PME event enable. 0: disable UART5 PME event. 1: enable UART5 PME event.
3	UART4_PME_EN	R/W	5VSB	0	UART 4 PME event enable. 0: disable UART 4 PME event. 1: enable UART 4 PME event.

2	UART3_PME_EN	R/W	5VSB	0	UART 3 PME event enable. 0: disable UART 3 PME event. 1: enable UART 3 PME event.
1	UART2_PME_EN	R/W	5VSB	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
0	UART1_PME_EN	R/W	5VSB	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.

5.8.18 PME Event Status 2 Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	RI2_PME_ST	R/WC	5VSB	-	RI2# PME event status. 0: RI2# has no PME event. 1: RI2# has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	RI1_PME_ST	R/WC	5VSB	-	RI1# PME event status. 0: RI1# has no PME event. 1: RI1# has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	UART6_PME_ST	R/WC	5VA	-	UART6 PME event status. 0: UART6 has no PME event. 1: UART6 has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	UART5_PME_ST	R/WC	5VA	-	UART5 PME event status. 0: UART5 has no PME event. 1: UART5 has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	UART4_PME_ST	R/WC	5VSB	-	UART 4 PME event status. 0: UART 4 has no PME event. 1: UART 4 has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	UART3_PME_ST	R/WC	5VSB	-	UART 3 PME event status. 0: UART 3 has no PME event. 1: UART 3 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UART2_PME_ST	R/WC	5VSB	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	UART1_PME_ST	R/WC	5VSB	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.

5.8.19 ACPI Control Register 1 — Index F4h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	VBAT	0	Reserved for Fintek test mode.
6	LAST_ST_MODE	R/W	VBAT	0	0: Last state is sampled by PWROK and RSMRST#. 1: Last state is sampled 1 second before AC lost.
5	EN_GPWAKEUP	R/W	VBAT	0	Set one to enable GPIO SMI event asserted via PWSOUT#.
4	EN_KBWAKEUP	R/W	VBAT	0	Set one to enable keyboard wakeup event asserted via PWSOUT#.
3	EN_MOWAKEUP	R/W	VBAT	0	Set one to enable mouse wakeup event asserted via PWSOUT#.
2-1	PWRCTRL	R/W	VBAT	11	The ACPI Control the PS_ON# to always on or always off or keep last state 00 : keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/WC	5VSB	1	When 5VSB power is lost, it will set to 1, and write 1 to clear it

5.8.20 ACPI Control Register 2 — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	5VSB	0	Reserved for future use.
6-5	PWROK_DELAY	R/W	5VSB	00b	The additional PWROK delay. 00: no delay (default) 01: 100ms. 10: 200ms 11: 400ms.
4-3	VDD_DELAY	R/W	5VSB	11b	The PWROK delay timing from VDD3VOK by following setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms (default)
2-0	Reserved	-	-	-	Reserved.

5.8.21 ACPI Control Register 3 — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	S3_SEL	R/W	5VSB	0	Select the KBC S3 condition source. 0: Enter S3 state when internal 3VCCOK signal is de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	PSON_DEL_EN	R/W	5VSB	0	0: PS_ON# is the inverted of S3# signal. 1: PS_ON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
5-4	Reserved	R/W	5VSB	0	Reserved for future use.

3	WDT_PWROK_EN	R/W	5VSB	0	Set “1” to enable WDTRST# via PWROK.
2-0	Reserved	R/W	5VSB	0	Reserved for future use.

5.8.22 LED Control Register 1 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	LED_VCC_INV_DIS	R/W	VBAT	0	Invert LED_VCC clock output.
6	LED_VCC_DS3	R/W	VBAT	0	Enable LED_VCC deep S3 mode. LED_VCC will output 0.25Hz clock with 75% duty when enter deep S3 state.
5-4	LED_VCC_S5_MODE	R/W	VBAT	0	Select LED_VCC mode in S5 state. The mode is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VCC_S3_MODE	R/W	VBAT	0	Select LED_VCC mode in S3 state. The mode is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
1-0	LED_VCC_S0_MODE	R/W	VBAT	0	Select LED_VCC mode in S0 state. The mode is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

5.8.23 LED Control Register 2 — Index F9h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PCIRST4_EN	R/W	VBAT	0	Set “1” to enable WDTRST# asserts via PCIRST4#.
6	LED_VSB_DS3	R/W	VBAT	0	0: Disable LED_VSB deep S3 mode. 1: Enable LED_VSB deep S3 mode. Output 0.25HZ clock with 25% duty.
5-4	LED_VSB_S5_MODE	R/W	VBAT	00	The three bits {LED_VSB_S5_MODE_ADD, LED_VSB_S5_MODE [1:0]} select the LED_VSB mode in S5 state. 000: Sink low. 001: Tri-state or drive high control by GPIO10_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.*
3-2	LED_VSB_S3_MODE	R/W	VBAT	00	The three bits {LED_VSB_S3_MODE_ADD, LED_VSB_S3_MODE [1:0]} select the LED_VSB mode in S3 state. 000: Sink low. 001: Tri-state or drive high control by GPIO10_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.*
1-0	LED_VSB_S0_MODE	R/W	VBAT	00	The three bits {LED_VSB_S0_MODE_ADD, LED_VSB_S0_MODE [1:0]} select the LED_VSB mode in S0 state. 000: Sink low. 001: Tri-state or drive high control by GPIO10_DRV_EN. 010: 0.5Hz clock with 50% duty. 011: 1Hz clock with 50% duty. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty.* 111: 0.25Hz clock with 25% duty.*

5.8.24 LED Control Register 3 — Index FAh

Bit	Name	R/W	Reset	Default	Description
7	LED_VSB_DRV_EN	R/W	VBAT	0	0: LED_VSB is open drain. 1: LED_VSB is push-pull.
6	LED_VSB_S5_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S5_MODE.

5	LED_VSB_S3_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S3_MODE.
4	LED_VSB_S0_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S0_MODE.
3	LED_VCC_DRV_EN	R/W	VBAT	0	0: LED_VCC is open drain. 1: LEC_VCC is push-pull.
2	LED_VCC_S5_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S5_MODE.
1	LED_VCC_S3_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S3_MODE.
0	LED_VCC_S0_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S0_MODE.

5.8.25 GPIO PME Register — Index FBh

Bit	Name	R/W	Reset	Default	Description
7	GPIO8_PME_ST	R/WC	5VSB	-	GPIO8 PME event status. 0: GPIO8 has no PME event. 1: GPIO8 has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	GPIO5_PME_ST	R/WC	5VSB	-	GPIO5 PME event status. 0: GPIO5 has no PME event. 1: GPIO5 has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	GPIO1_PME_ST	R/WC	5VSB	-	GPIO1 PME event status. 0: GPIO1 has no PME event. 1: GPIO1 has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	GPIO0_PME_ST	R/WC	5VSB	-	GPIO0 PME event status. 0: GPIO0 has no PME event. 1: GPIO0 has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	GPIO8_PME_EN	R/W	5VSB	0	GPIO8 PME event enable. 0: disable GPIO8 PME event. 1: enable GPIO8 PME event.
2	GPIO5_PME_EN	R/W	5VSB	0	GPIO5 PME event enable. 0: disable GPIO5 PME event. 1: enable GPIO5 PME event.
1	GPIO1_PME_EN	R/W	5VSB	0	GPIO1 PME event enable. 0: disable GPIO1 PME event. 1: enable GPIO1 PME event.
0	GPIO0_PME_EN	R/W	5VSB	0	GPIO0 PME event enable. 0: disable GPIO0 PME event. 1: enable GPIO0 PME event.

5.8.26 DSW Delay Register — Index FCh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3-0	DSW_DELAY	R/W	5VSB	7h	This is the delay time between SUS_WARN# and SUS_ACK#. The unit is 0.5 sec. Default time is 3.5s ~ 4s. The default could be trimmed to 0s ~ 0.5s.

5.8.27 ACPI Control Register 4 — Index FDh

Bit	Name	R/W	Reset	Default	Description
7	BOOT_FAIL_PD_DIS	R/W	VBAT	0	Set “1” to disable power down when boot fail.
6	PWSIN_4S_PD_EN	R/W	VBAT	0	Set ”1” to enable power down by pressing PWSIN# over 4 second.
5-0	BOOT_FAIL_PD_DIS	R/W	VBAT	0	Reserved

5.8.28 RI De-bounce Select Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved
1-0	RI_DB_SEL	R/W	5VSB	0	Select RI# de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

5.9 eSPI to LPC (E2L) Device Configuration Registers (LDN CR0E) (F81967 Only)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	ESPI to LPC Device Enable Register	-	-	-	-	-	-	-	0
F0	Address Decode 1 High Byte	0	0	0	0	0	0	0	0
F1	Address Decode 1 Low Byte	0	0	0	0	0	0	0	0
F2	Address Decode 2 High Byte	0	0	0	0	0	0	0	0
F3	Address Decode 2 Low Byte	0	0	0	0	0	0	0	0
F4	Address Decode 3 High Byte	0	0	0	0	0	0	0	0
F5	Address Decode 3 Low Byte	0	0	0	0	0	0	0	0
F6	Address Decode 4 High Byte	0	0	0	0	0	0	0	0
F7	Address Decode 4 Low Byte	0	0	0	0	0	0	0	0
F8	ESPI to LPC Control Register	0	0	0	0	0	0	0	0
F9	ESPI to LPC Control Register	0	0	0	0	0	0	1	0
FE	SIRQ Enable Register 1	0	0	0	0	0	0	0	0
FF	SIRQ Enable Register 2	0	0	0	0	0	0	0	0

5.9.1 ESPI to LPC Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	E2L_EN	R/W	5VSB	0	0: disable eSPI to LPC. 1: enable eSPI to LPC.

5.9.2 Address Decode 1 High Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7-0	ADDR_DEC1_HI	R/W	5VSB	0h	Address decode range 1 for eSPI to LPC. The range is 32-byte.

5.9.3 Address Decode 1 Low Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7-0	ADDR_DEC1_LO	R/W	5VSB	0h	Address decode range 1 for eSPI to LPC. The range is 32-byte.

5.9.4 Address Decode 2 High Register — Index F2h

Bit	Name	R/W	Reset	Default	Description

7-0	ADDR_DEC2_HI	R/W	5VSB	0h	Address decode range 2 for eSPI to LPC. The range is 32-byte.

5.9.5 Address Decode 2 Low Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7-0	ADDR_DEC2_LO	R/W	5VSB	0h	Address decode range 2 for eSPI to LPC. The range is 32-byte.

5.9.6 Address Decode 3 High Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	ADDR_DEC3_HI	R/W	5VSB	0h	Address decode range 3 for eSPI to LPC. The range is 32-byte.

5.9.7 Address Decode 3 Low Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-0	ADDR_DEC3_LO	R/W	5VSB	0h	Address decode range 3 for eSPI to LPC. The range is 32-byte.

5.9.8 Address Decode 4 High Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7-0	ADDR_DEC4_HI	R/W	5VSB	0h	Address decode range 4 for eSPI to LPC. The range is 32-byte.

5.9.9 Address Decode 4 Low Register — Index F7h

Bit	Name	R/W	Reset	Default	Description
7-0	ADDR_DEC4_LO	R/W	5VSB	0h	Address decode range 4 for eSPI to LPC. The range is 32-byte.

5.9.10 ESPI to LPC Control Register—Index F8h

Bit	Name	R/W	Reset	Default	Description
7	SIRQ_MODE	R/W	5VSB	0h	Select SIRQ Mode. 0: Continuous mode. 1: Quiet mode.
6	E2L_DUMMY	R/W	5VSB	0h	Dummy register for future use.
5	ADDR_DEC4_EN	R/W	5VSB	0h	0: Disable Address Decode 4. 1: Enable Address Decode 4.
4	ADDR_DEC3_EN	R/W	5VSB	0h	0: Disable Address Decode 4. 1: Enable Address Decode 4.

3	ADDR_DEC2_EN	R/W	5VSB	0h	0: Disable Address Decode 4. 1: Enable Address Decode 4.
2	ADDR_DEC1_EN	R/W	5VSB	0h	0: Disable Address Decode 4. 1: Enable Address Decode 4.
1	E2L_4E_EN	R/W	5VSB	0h	0: Disable 0x4E/0x4F decode. 1: Enable 0x4E/0x4F decode.
0	E2L_2E_EN	R/W	5VSB	0h	0: Disable 0x2E/0x2F decode. 1: Enable 0x2E/0x2F decode.

5.9.11 ESPI to LPC Control Register—Index F9h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved
5-4	M_LCLK_F_SEL	R/W	5VSB	0h	LCLK Frequency Select 1x: Follow CLKIN 01: 32MHz. 00: 24MHz.
3	Reserved	-	-	-	Reserved
2-0	M_LCLK_PHASE	R/W	5VSB	2h	This register is used to fine tune M_LCLK phase.

5.9.12 SIRQ Enable Register 1 — Index FEh

Bit	Name	R/W	Reset	Default	Description
7	E2L_IRQ15_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ15. 1: Enable SIRQ to eSPI IRQ15.
6	E2L_IRQ14_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ14. 1: Enable SIRQ to eSPI IRQ14.
5	E2L_IRQ13_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ13. 1: Enable SIRQ to eSPI IRQ13.
4	E2L_IRQ12_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ12. 1: Enable SIRQ to eSPI IRQ12.
3	E2L_IRQ11_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ11. 1: Enable SIRQ to eSPI IRQ11.
2	E2L_IRQ10_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ10. 1: Enable SIRQ to eSPI IRQ10.
1	E2L_IRQ9_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ9. 1: Enable SIRQ to eSPI IRQ9.
0	E2L_IRQ8_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ8. 1: Enable SIRQ to eSPI IRQ8.

5.9.13 IRQ Enable Register 2 — Index FFh

Bit	Name	R/W	Reset	Default	Description
7	E2L_IRQ7_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ7. 1: Enable SIRQ to eSPI IRQ7.
6	E2L_IRQ6_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ6. 1: Enable SIRQ to eSPI IRQ6.
5	E2L_IRQ5_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ5. 1: Enable SIRQ to eSPI IRQ5.
4	E2L_IRQ4_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ4. 1: Enable SIRQ to eSPI IRQ4.
3	E2L_IRQ3_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ3. 1: Enable SIRQ to eSPI IRQ3.
2	E2L_IRQ2_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ2. 1: Enable SIRQ to eSPI IRQ2.
1	E2L_IRQ1_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ1. 1: Enable SIRQ to eSPI IRQ1.
0	E2L_IRQ0_EN	R/W	5VSB	0h	0: Disable SIRQ to eSPI IRQ0. 1: Enable SIRQ to eSPI IRQ0.

5.10 SPI Master Device Configuration Registers (LDN CR0F)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB LSB							
F1	Write Register	0	0	0	0	0	0	0	0
F2	Continuous Write Register	0	0	0	0	0	0	0	0
F3	SPI Status Register	0	-	-	-	-	0	0	0
F4	SPI Read Data	0	0	0	0	0	0	0	0
F5	SPI Control Register	0	0	0	0	0	0	0	0
F6	SPI Clock Divisor	0	0	0	0	0	0	1	1

5.10.1 Write Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7-0	WR_DATA	R/W	5VSB	0	Write this bit will 1. Set SPI_WR_STS, 2. Assert CS#. 3. 8-bit clock with the written data. 4. De-assert CS#.

5.10.2 Continuous Write Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-0	CONT_WR_DATA	R/W	5VSB	0	Write this bit will 1. Set SPI_CONT_WR_STS. 2. Assert CS#. 3. 8-bit clock with the written data. 4. Keep asserting CS#.

5.10.3 SPI Status Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	R/W	5VSB	0h	Dummy register for future use.
6-3	Reserved	-	5VSB	-	Reserved.
2	SPI_END	R/WC	5VSB	0	This bit is set when the command is finished. Write “1” to clear this bit.
1	SPI_CONT_WR_STS	R	5VSB	0	This bit is set when the CONT_WR_DATA is written and auto clear after data is sent.
0	SPI_WR_STS	R	5VSB	0	This bit is set when WR_DATA is written and auto clear after data is sent.

5.10.4 SPI Read Data Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SPI_Read	R/W	5VSB	0h	The read data of SPI.

5.10.5 SPI Control Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	SPI_CS_DIS	R/W	5VSB	0h	Set “1” to disable SPI_CS#.
6-2	Reserved	R/W	5VSB	0h	Dummy register for future use.
1	CPHA	R/W	5VSB	0h	0: Trailing edge to transmit data. 1: Leading edge to transmit data.
0	CPOL	R/W	5VSB	0h	0: SPI_CLK hold on low. 1: SPI_CLK hold on high.

5.10.6 SPI Clock Divisor Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7-0	CLK_DIV	R/W	5VSB	0h	SPI_CLK divisor. SPI_CLK is calculated by 48MHz/(CLK_DIV+1)

5.11 UART1 Device Configuration Registers (LDN CR10)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART1 Device Enable Register	-	-	-	-	-	-	-	1
60	UART1 Base Address High Register	0	0	0	0	0	0	1	1
61	UART1 Base Address Low Register	1	1	1	1	1	0	0	0
70	UART1 IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	UART1 IRQ Share Register	0	0	0	0	-	-	0	0
F2	UART1 Clock Source Select Register	-	-	-	-	-	-	0	0
F4	UART1 9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	UART1 9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	UART1 FIFO Select Register	0	0	0	0	0	0	0	0
F7	UART1 Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	UART1 Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART1 LED Enable Register	-	-	-	-	-	-	0	0
FF	UART1 9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

5.11.1 UART1 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	COM1_EN	R/W	LRESET#	1	0: disable UART 1 I/O Port. 1: enable UART 1 I/O Port.

5.11.2 UART1 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of UART 1 base address.

5.11.3 UART1 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	F8h	The LSB of UART 1 base address.

5.11.4 UART1 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description

7-4	Reserved	-	-	-	Reserved.
3-0	SELUR1IRQ	R/W	LRESET#	4h	Select the IRQ channel for UART 1.

5.11.5 UART1 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LREST#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART1 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

5.11.6 UART1 Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART1_CLK_SEL	R/W	LRESET#	0	Select the clock source for UART1. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.11.7 UART1 9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 1. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 2. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.11.8 UART1 9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 3. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 4. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.11.9 UART1 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.

5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LREST#	0	IRQ_MODE1 and IRQ_MODE0 (UART1 IRQ Share Register — Index F0h, bit1) will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART1 IRQ share register— index F0h, bit 0).
2	Reserved	R/W	LREST#	0	Dummy register for future use.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

5.11.10 UART1 Auto Flow Control Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W	LRESET#	00h	Threshold for RX to request data via RTS# or DTR#. When RX FIFO is under this threshold, RX asserts RTS# or DTR# to request new data.

5.11.11 UART1 Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW _PIN_SEL	R/W	LRESET#	0	Select pin for auto flow control. 0: DTR#. 1: RTS#.
6-0	XOFF_THR	R/W	LRESET#	00h	When RX FIFO is over this threhold, RX de-asserts RTS# or DTR# to inform TX stoping to transmit data.

5.11.12 UART1 LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	TX_LED_EN	R/W	LRESET#	0	Set “1” to enable TX LED via DTR#. When a data is sent, a 50-ms pulse is output via DTR#. The max freq. is 5Hz.

5.11.13 UART1 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

5.12 UART2 Device Configuration Registers (LDN CR11)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB LSB							
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1
60	UART2 Base Address High Register	0	0	0	0	0	0	1	0
61	UART2 Base Address Low Register	1	1	1	1	1	0	0	0
70	UART2 IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	UART2 IRQ Share Register	0	0	0	0	-	-	0	0
F2	UART2 Clock Source Select Register	-	-	-	-	-	-	0	0
F4	UART2 9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	UART2 9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	UART2 FIFO Select Register	0	0	0	0	0	0	0	0
F7	UART2 Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	UART2 Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART2 LED Enable Register	-	-	-	-	-	-	0	0
FF	UART2 9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

5.12.1 UART2 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	COM2_EN	R/W	LRESET#	1	0: disable UART 2 I/O Port. 1: enable UART 2 I/O Port.

5.12.2 UART2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	02h	The MSB of UART 2 base address.

5.12.3 UART2 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-1	BASE_ADDR_LO	R/W	LRESET#	F8h	The LSB of UART 2 base address.

5.12.4 UART2 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUR12RQ	R/W	LRESET#	3h	Select the IRQ channel for UART 2.

5.12.5 UART2 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART2 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART2 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

5.12.6 UART2 Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART2_CLK_SEL	R/W	LRESET#	0	Select the clock source for UART2. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.12.7 UART2 9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 5. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 6. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.12.8 UART2 9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 7. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 8. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.12.9 UART2 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.

5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 (UART2 IRQ Share Register — Index F0h, bit1) will select the UART2 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART2 IRQ share register— index F0h, bit 0).
2	Reserved	-	LRESET#	-	Reserved.
1-0	FIFO_MODE	R/W	LREST#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

5.12.10 UART2 Auto Flow Control Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W	LRESET#	00h	Threshold for RX to request data via RTS# or DTR#. When RX FIFO is under this threshold, RX asserts RTS# or DTR# to request new data.

5.12.11 UART2 Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW _PIN_SEL	R/W	LRESET#	0	Select pin for auto flow control. 0: DTR#. 1: RTS#.
6-0	XOFF_THR	R/W	LRESET#	00h	When RX FIFO is over this threhold, RX de-asserts RTS# or DTR# to inform TX stoping to transmit data.

5.12.12 UART2 LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.

1	TX_LED_EN	R/W	LRESET#	0	Set “1” to enable TX LED via DTR#. When a data is sent, a 50-ms pulse is output via DTR#. The max freq. is 5Hz.
0	XOFF_THR	R/W	LRESET#	0	Set “1” to enable RX LED via DSR#. When a data is received, a 50-ms pulse is output via DSR#. The max freq. is 5Hz.

5.12.13 UART2 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

5.13 UART3 Device Configuration Registers (LDN CR12)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART3 Device Enable Register	-	-	-	-	-	-	-	0
60	UART3 Base Address High Register	0	0	0	0	0	0	1	1
61	UART3 Base Address Low Register	1	1	1	0	1	0	0	0
70	UART3 IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	UART3 IRQ Share Register	0	0	0	0	-	-	0	0
F2	UART3 Clock Source Select Register	-	-	-	-	-	-	0	0
F4	UART3 9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	UART3 9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	UART3 FIFO Select Register	0	0	0	0	0	0	0	0
F7	UART3 Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	UART3 Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART3 LED Enable Register	-	-	-	-	-	-	0	0
FF	UART3 9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

5.13.1 UART3 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	COM3_EN	R/W	LRESET#	0	0: disable UART 3 I/O Port. 1: enable UART 3 I/O Port.

5.13.2 UART3 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of UART 3 base address.

5.13.3 UART3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	E8h	The LSB of UART 3 base address.

5.13.4 UART3 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART3IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 3.

5.13.5 UART3 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART3 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART3 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

5.13.6 UART3 Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART3_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART3. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.13.7 UART3 9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 9. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 10. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.13.8 UART3 9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 11. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 12. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.13.9 UART3 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.

5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 (UART3 IRQ Share Register — Index F0h, bit1) will select the UART3 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART3 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

5.13.10 UART3 Auto Flow Control Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W	LRESET#	00h	Threshold for RX to request data via RTS# or DTR#. When RX FIFO is under this threshold, RX asserts RTS# or DTR# to request new data.

5.13.11 UART3 Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW _PIN_SEL	R/W	LRESET#	0	Select pin for auto flow control. 0: DTR#. 1: RTS#.
6-0	XOFF_THR	R/W	LRESET#	00h	When RX FIFO is over this threhold, RX de-asserts RTS# or DTR# to inform TX stoping to transmit data.

5.13.12 UART3 LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.

1	TX_LED_EN	R/W	LRESET#	0	Set “1” to enable TX LED via DTR#. When a data is sent, a 50-ms pulse is output via DTR#. The max freq. is 5Hz.
0	XOFF_THR	R/W	LRESET#	0	Set “1” to enable RX LED via DSR#. When a data is received, a 50-ms pulse is output via DSR#. The max freq. is 5Hz.

5.13.13 UART3 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

5.14 UART4 Device Configuration Registers (LDN CR13)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB LSB							
30	UART4 Device Enable Register	0	0	0	0	0	0	0	0
60	UART4 Base Address High Register	0	0	0	0	0	0	1	0
61	UART4 Base Address Low Register	1	1	1	0	1	0	0	0
70	UART4 IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	UART4 IRQ Share Register	0	0	0	0	-	-	0	0
F2	UART4 Clock Source Select Register	-	-	-	-	-	-	0	0
F4	UART4 9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	UART4 9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	UART4 FIFO Select Register	0	0	0	0	0	0	0	0
F7	UART4 Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	UART4 Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART4 LED Enable Register	-	-	-	-	-	-	0	0
FF	UART4 9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

5.14.1 UART4 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	COM4_EN	R/W	LRESET#	0	0: disable UART 4 I/O Port. 1: enable UART 4 I/O Port.

5.14.2 UART4 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	02h	The MSB of UART 4 base address.

5.14.3 UART4 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	E8h	The LSB of UART 4 base address.

5.14.4 UART4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART4IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 4.

5.14.5 UART4 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	LRESET#	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART4 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART4 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

5.14.6 Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART4_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART4. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.14.7 UART4 9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 13. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 14. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.14.8 UART4 9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 15. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 16. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.14.9 UART4 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.

5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 (UART4 IRQ Share Register — Index F0h, bit1) will select the UART4 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART4 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

5.14.10 UART4 Auto Flow Control Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W	LRESET#	00h	Threhold for RX to request data via RTS# or DTR#. When RX FIFO is under this threhold, RX asserts RTS# or DTR# to request new data.

5.14.11 UART4 Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_PIN_SEL	R/W	LRESET#	0	Select pin for auto flow control. 0: DTR#. 1: RTS#.
6-0	XOFF_THR	R/W	LRESET#	00h	When RX FIFO is over this threhold, RX de-assert RTS# or DTR# to inform TX stoping to transmit data.

5.14.12 UART4 LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.

1	TX_LED_EN	R/W	LRESET#	0	Set “1” to enable TX LED via DTR#. When a data is sent, a 50-ms pulse is output via DTR#. The max freq. is 5Hz.
0	XOFF_THR	R/W	LRESET#	0	Set “1” to enable RX LED via DSR#. When a data is received, a 50-ms pulse is output via DSR#. The max freq. is 5Hz.

5.14.13 UART4 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

5.15 UART5 Device Configuration Registers (LDN CR14)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART5 Device Enable Register	-	-	-	-	-	-	-	0
60	UART5 Base Address High Register	0	0	0	0	0	0	0	0
61	UART5 Base Address Low Register	0	0	0	0	0	0	0	0
70	UART5 IRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	UART5 IRQ Share Register	0	0	0	0	-	-	0	0
F2	UART5 Clock Source Select Register	-	-	-	-	-	-	0	0
F4	UART5 9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	UART5 9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	UART5 FIFO Select Register	0	0	0	0	0	0	0	0
F7	UART5 Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	UART5 Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART5 LED Enable Register	-	-	-	-	-	-	0	0
FF	UART5 9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

5.15.1 UART5 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	COM5_EN	R/W	LRESET#	0	0: disable UART 5 I/O Port. 1: enable UART 5 I/O Port.

5.15.2 UART5 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of UART 5 base address.

5.15.3 UART5 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	The LSB of UART 5 base address.

5.15.4 UART5 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART5IRQ	R/W	LRESET#	0h	Select the IRQ channel for UART 5.

5.15.5 UART5 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3-2	Reserved	-	LRESET#	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART5 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART5 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

5.15.6 UART5 Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART5_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART5. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.15.7 UART5 9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 17. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 18. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.15.8 UART5 9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 19. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 20. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.15.9 UART5 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.

5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 (UART5 IRQ Share Register — Index F0h, bit1) will select the UART5 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART5 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

5.15.10 UART5 Auto Flow Control Register 1 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W	LRESET#	00h	Threhold for RX to request data via RTS# or DTR#. When RX FIFO is under this threhold, RX asserts RTS# or DTR# to request new data.

5.15.11 UART5 Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW _PIN_SEL	R/W	LRESET#	0	Auto Flow Control pin pair select: 0: DTR#. 1: RTS#.
6-0	XOFF_THR	R/W	LRESET#	00h	When RX FIFO is over this threhold, RX de-asserts RTS# or DTR# to inform TX stoping to transmit data.

5.15.12 UART5 LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.

1	TX_LED_EN	R/W	LRESET#	0	Set “1” to enable TX LED via DTR#. When a data is sent, a 50-ms pulse is output via DTR#. The max freq. is 5Hz.
0	XOFF_THR	R/W	LRESET#	0	Set “1” to enable RX LED via DSR#. When a data is received, a 50-ms pulse is output via DSR#. The max freq. is 5Hz.

5.15.13 UART5 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

5.16 UART6 Device Configuration Registers (LDN CR15)

"-" Reserved or Tri-State

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART6 Device Enable Register	-	-	-	-	-	-	-	0
60	UART6 Base Address High Register	0	0	0	0	0	0	0	0
61	UART6 Base Address Low Register	0	0	0	0	0	0	0	0
70	UART6 IRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	UART6 IRQ Share Register	0	0	0	0	-	-	0	0
F2	UART6 Clock Source Select Register	-	-	-	-	-	-	0	0
F4	UART6 9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	UART6 9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	UART6 FIFO Select Register	0	0	0	0	0	0	0	0
F7	UART6 Auto Flow Control Register 1	0	0	0	0	0	0	0	0
F8	UART6 Auto Flow Control Register 2	0	0	0	0	0	0	0	0
FE	UART6 LED Enable Register	-	-	-	-	-	-	0	0
FF	UART6 9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

5.16.1 UART6 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	COM6_EN	R/W	LRESET#	0	0: disable UART 6 I/O Port. 1: enable UART 6 I/O Port.

5.16.2 UART6 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of UART 6 base address.

5.16.3 UART6 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	The LSB of UART 6 base address.

5.16.4 UART6 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUART6IRQ	R/W	LRESET#	0h	Select the IRQ channel for UART 6.

5.16.5 UART6 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise is kept low.
3	RXW4C_IR	R/W	LRESET#	0	0 : No reception delay when SIR is changed from TX to RX. 1 : Reception delay 4 character-time when SIR is changed from TX to RX.
2	TXW4C_IR	R/W	LRESET#	0	0 : No transmission delay when SIR is changed from RX to TX. 1 : Transmission delay 4 character-time when SIR is changed from RX to TX.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART6 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0will select the UART6 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.

5.16.6 UART6 IR Mode Select Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved. Return 010b when read.

4-3	IRMODE1 IRMODE0	R/W	LRESET#	00b	0X: Disable IR1 function. 10 : Enable IR1 function, active pulse is 1.6uS. 11 : Enable IR1 function, active pulse is 3/16 bit time.
2	HDUPLX	R/W	LRESET#	1	0 : Full Duplex function for IR self test. 1 : Half Duplex function. Return 1 when read.
1	TXINV_IR	R/W	LRESET#	0	0 : IRTX is not inversed. 1 : Inverse the IRTX.
0	RXINV_IR	R/W	LRESET#	0	0: IRRX is not inversed. 1: Inverse the IRRX.

5.16.7 UART6 Clock Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UART6_CLK_SEL	R/W	LRESET#	00b	Select the clock source for UART6. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.16.8 UART6 9bit-mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 21. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 22. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.16.9 UART6 9bit-mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7:0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 23. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 24. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

5.16.10 UART6 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LRESET#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LRESET#	0	IRQ_MODE1 and IRQ_MODE0 (UART6 IRQ Share Register — Index F0h, bit1) will select the UART6 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART6 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

5.16.11 UART6 Auto Flow Control Register 1— Index F7h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_EN	R/W	LRESET#	0	0: Disable Auto Flow Control. 1: Enable Auto Flow Control.
6-0	XON_THR	R/W	LRESET#	00h	Threhold for RX to request data via RTS# or DTR#. When RX FIFO is under this threhold, RX asserts RTS# or DTR# to request new data.

5.16.12 UART6 Auto Flow Control Register 2 — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	AUTO_FLOW_PIN_SEL	R/W	LRESET#	0	Select pin for auto flow control. 0: DTR#. 1: RTS#.
6-0	XOFF_THR	R/W	LRESET#	00h	When RX FIFO is over this threhold, RX de-asserts RTS# or DTR# to inform TX stoping to transmit data.

5.16.13 UART6 LED Enable Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1	TX_LED_EN	R/W	LRESET#	0	Set “1” to enable TX LED via DTR#. When a data is sent, a 50-ms pulse is output via DTR#. The max freq. is 5Hz.
0	XOFF_THR	R/W	LRESET#	0	Set “1” to enable RX LED via DSR#. When a data is received, a 50-ms pulse is output via DSR#. The max freq. is 5Hz.

5.16.14 UART6 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	-40 ~ +85	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may dversely affect the life and reliability of the device.

6.2 DC Characteristics

(Ta = 0° C to 70° C, 3VCC = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Operating Voltage	VDD	3.0	3.3	3.6	V	
Battery Voltage	VBAT	2.4	3.3	3.6	V	
Operating Current	ICC		10		mA	3VCC=3.3V VBAT=3.3V
Idle State Current	ISTY		5		uA	3VCC=3.3V VBAT=3.3V
Battery Current	IBAT		4		uA	3VCC=3.3V VBAT=3.3V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
$I/O_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/O_{16t,u47k}$-TTL level bi-directional pin with 16 mA source-sink capability, internal pull-up 47kΩ						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{14st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 14mA source-sink capability, 5V tolerance.						

Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-14	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+14		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD$_{8st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 8mA source-sink capability, 5V tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-8	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+8		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD$_{12st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 12mA source-sink capability, 5V tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD$_{24st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 24mA source-sink capability, 5V tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-24	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+24		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN$_{st}$ - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
IN$_{st,5v}$ - TTL level input pin with schmitt trigger, 5V tolerance						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
IN$_{st,lv}$ - TTL level input pin with schmitt trigger, low level.						
Input Low Voltage	VIL			0.6	V	

Input High Voltage	VIH	0.9			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{t,u47,5v}$ - TTL level input pin, internal pull-up 47Ω, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	0.2			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{t,5v}$ - TTL level input pin, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	0.2			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
I_{lv}/O_{lv} - TTL level input/output pin with schmitt trigger, low level.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$OD_{12,5v}$-Open-drain output with12 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{24,5v}$-Open-drain output with24 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-24		mA	VOL = 0.4V
$OD_{16,u10k,5v}$-Open-drain output with 16 mA sink capability, pull-up 10kΩ, 5V tolerance.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
$OD_{16,u10}$-Open-drain output with 16 mA sink capability, pull-up 10kΩ.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
$OOD_{12,5v}$-Open drian or push pull by the register, with 12 mA source/sink capability, 5V tolerance.						
Output High Current	IOH		-12		mA	VOH = 0.4V
Output Low Current	IOL		+12		mA	VOL = 0.4V
O_{12}- Output pin with 12 mA source-sink capability.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
O_{16}- Output pin with 16 mA source-sink capability.						
Output High Current	IOH		+16		mA	VOH = 2.4V
$O_{16,5v}$- Output pin with 16 mA source-sink capability, 5V tolerance.						
Output High Current	IOH		+16		mA	VOH = 2.4V
O_{18}- Output pin with 18 mA source-sink capability.						
Output High Current	IOH		+18		mA	VOH = 2.4V
O_{8}- Output pin with 8 mA source-sink capability.						
Output High Current	IOH		+8		mA	VOH = 2.4V
O_{30}- Output pin with 30 mA source-sink capability.						
Output High Current	IOH	+26	+30		mA	VOH = 2.4V

O_{14}- Output pin with 14 mA source-sink capability, 5V tolerance.						
Output High Current	IOH		+14		mA	VOH = 2.4V
I_{LV}/$O_{D8,s1}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+8		mA	VOH = 1.0V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0 V
I/$OD_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0V
I/$OD_{16st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0V
I_{IV} /$OD_{16st,5v}$-Low level bi-directional pin with schmitt trigger, Open-drain output with16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0V

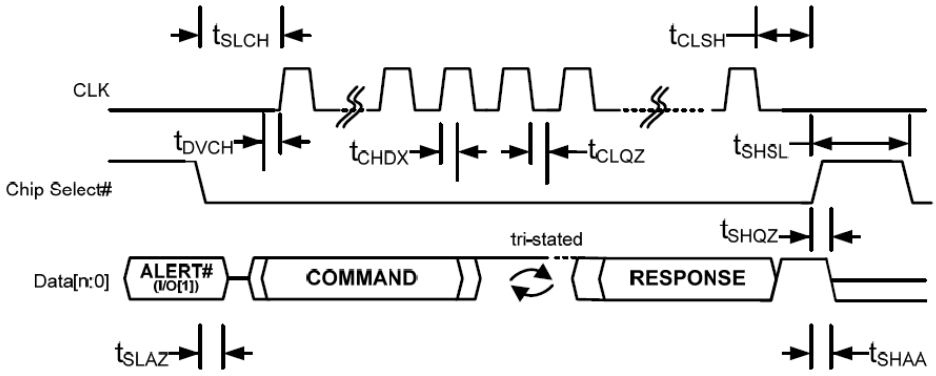
6.3 eSPI Interface

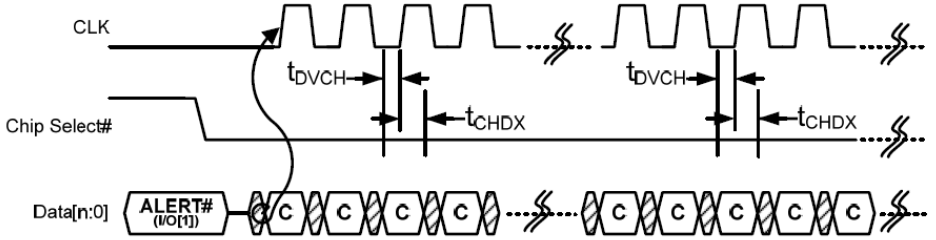
SYMBOL	DESCRIPTION
t_{CKH}	Clock High Time

t_{CKL}	Clock Low Time
t_{SLCH}	Chip Select# Setup Time
t_{CLSH}	Chip Select# Hold Time
t_{SHSL}	Chip Select# De-assertion Time
t_{DVCH}	Data In Setup Time
t_{CHDX}	Data In Hold Time
t_{CLQZ}	Output Disable Time during Turn-Around
t_{CLQV}	Output Data Valid Time
t_{CLQX}	Output Data Hold Time
t_{SHQZ}	Output Disable Time after Chip Select# De-assertion
t_{SLAZ}	Chip Select# Assertion to I/O[1] or ALERT# Tri-stated
t_{SHAA}	Chip Select# De-assertion to I/O[1] or ALERT# Assertion
t_{INIT}	eSPI Reset# De-assertion to First Transaction (GET_CONFIGURATION)
$t_{INIT-FREQ}$	Initial Bus Frequency upon eSPI Reset# De-assertion

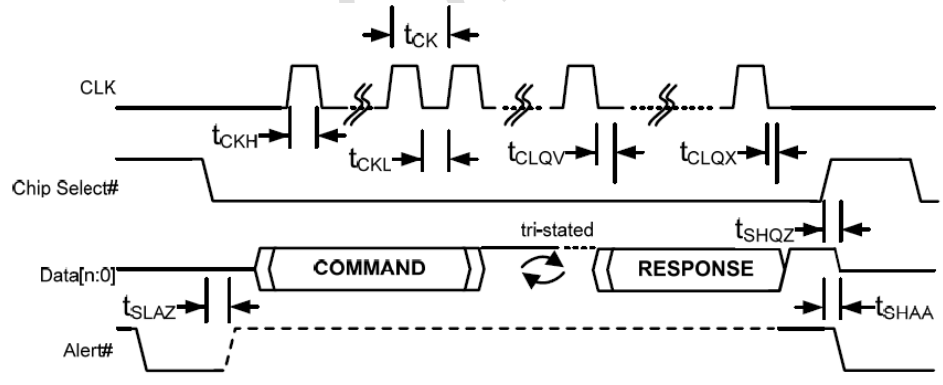
SYMBOL	20MHZ		25MHZ		33MHZ		50MHZ		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK}	50		40		30		20		ns
t_{CKH}	0.4		0.4		0.4		0.4		t_{CK}
t_{CKL}	0.4		0.4		0.4		0.4		t_{CK}
t_{SLCH}	75		60		45		30		ns
t_{CLSH}	50		40		30		20		ns
t_{SHSL}	50		40		30		20		ns
t_{DVCH}	12		10		7		5		ns
t_{CHDX}	12		10		7		5		ns
t_{CLQZ}		15		12		9		8	ns
t_{CLQV}		20		15		10		8	ns
t_{CLQX}	0		0		0		0		ns
t_{SHQZ}		15		12		9		8	ns
t_{SLAZ}		15		12		9		8	ns
t_{SHAA}	15		12		9		8		ns
t_{INIT}	1		1		1		1		µs
$t_{INIT-FREQ}$		20		20		20		20	MHz

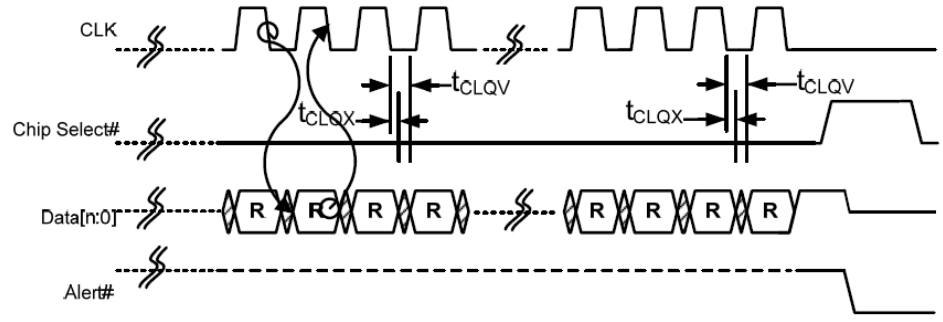
Input Timing Diagram





Output Timing Diagram

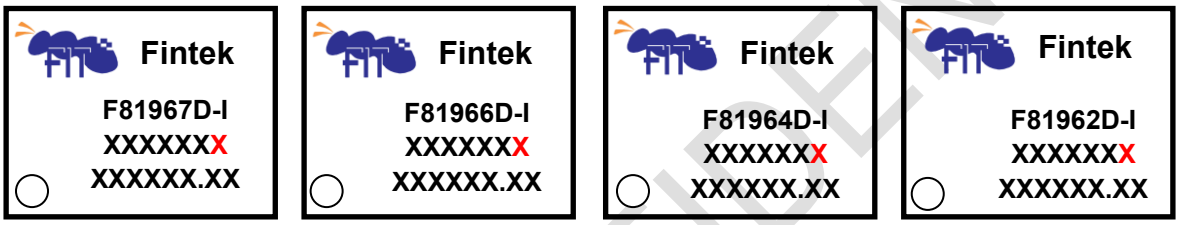




7 Ordering Information

Part Number	Package Type
F81967D-I	128-LQFP (Green Package)
F81966D-I	128-LQFP (Green Package)
F81964D-I	128-LQFP (Green Package)
F81962D-I	128-LQFP (Green Package)

8 Top Marking Specification



1st Line: Fintek Logo

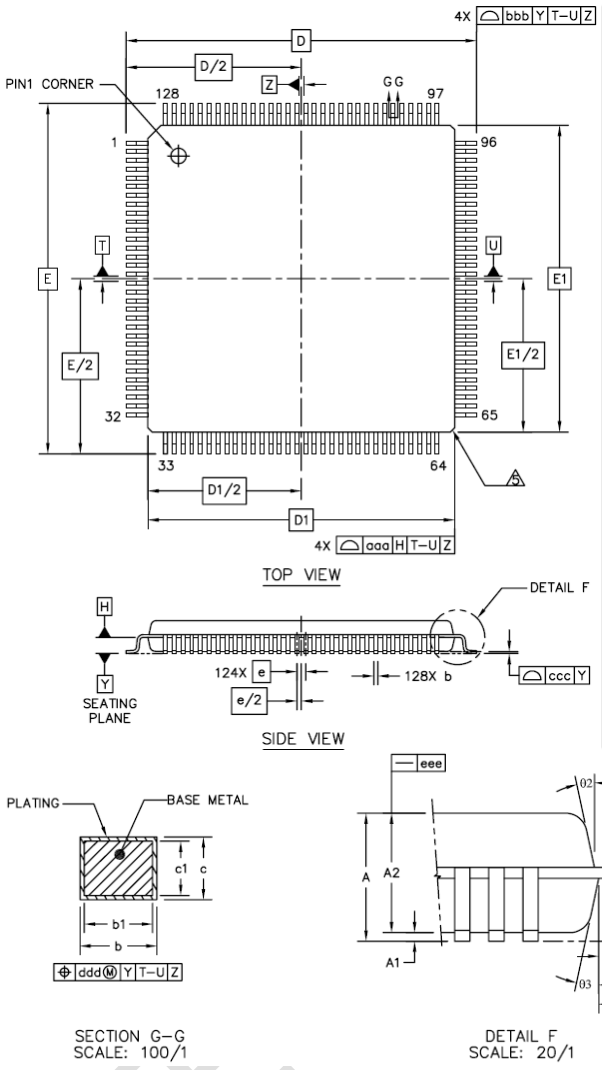
2nd Line: Device Name → **F81962D-I,** where D means 128-LQFP & -I means the industrial spec.
F81964D-I, where D means 128-LQFP & -I means the industrial spec.
F81966D-I, where D means 128-LQFP & -I means the industrial spec.
F81967D-I, where D means 128-LQFP & -I means the industrial spec.

3rd Line: Assembly Plant Code (X) + Assembled Year Code (X) + Week Code (XX) + Fintek Internal Code (XX) + IC Version (X) where A means version A, B means version B, …

4th Line: Wafer Fab Code (XXXX…XX)

◯ : Pin 1 Identifier

9 Package Dimensions (128-LQFP)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

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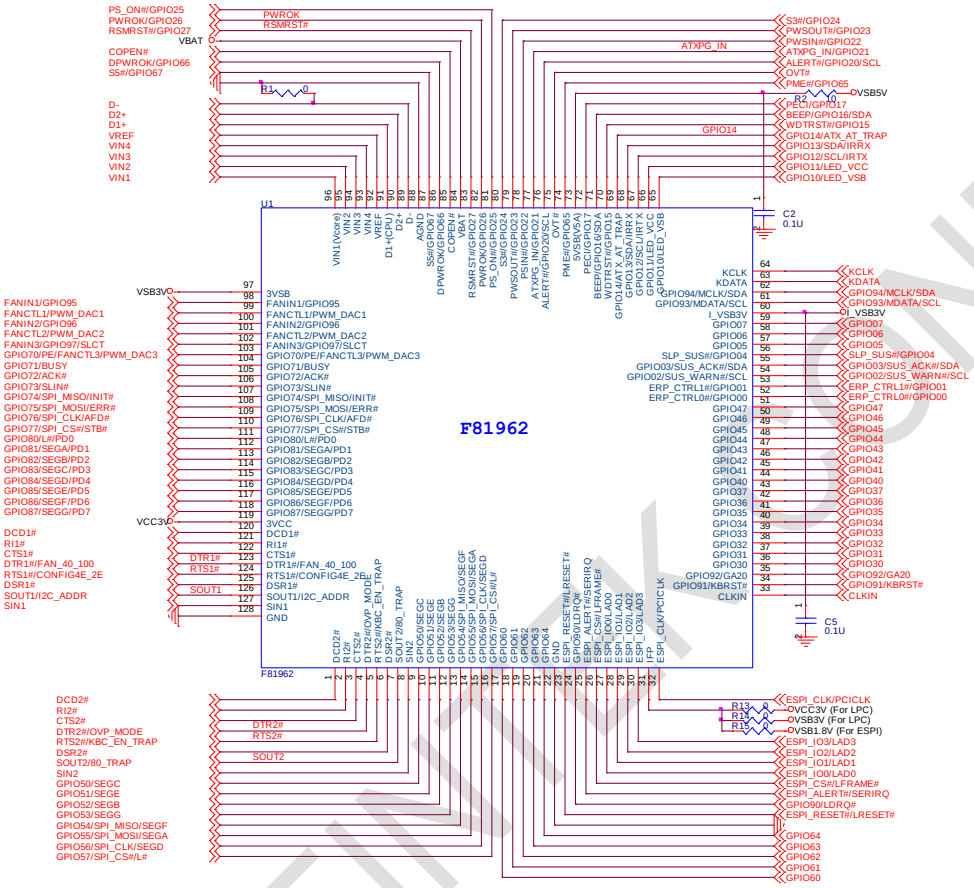
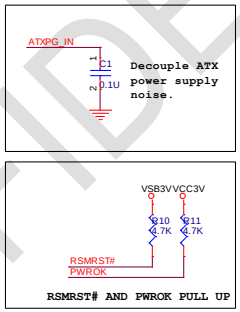
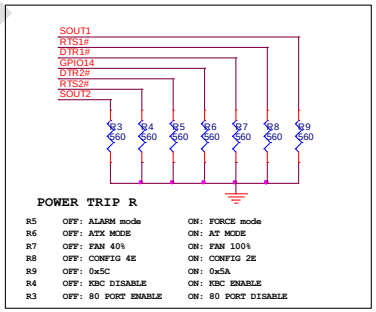
FAX : 866-2-8227-8037

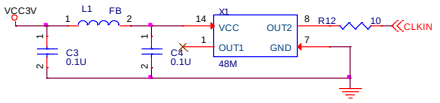
10 ApplicationCircuit

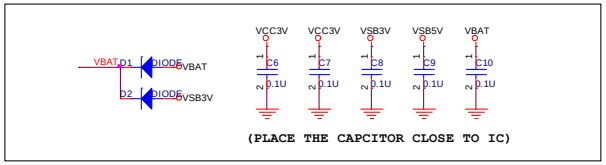
F81962/F81964/F81966 Demo Circuit











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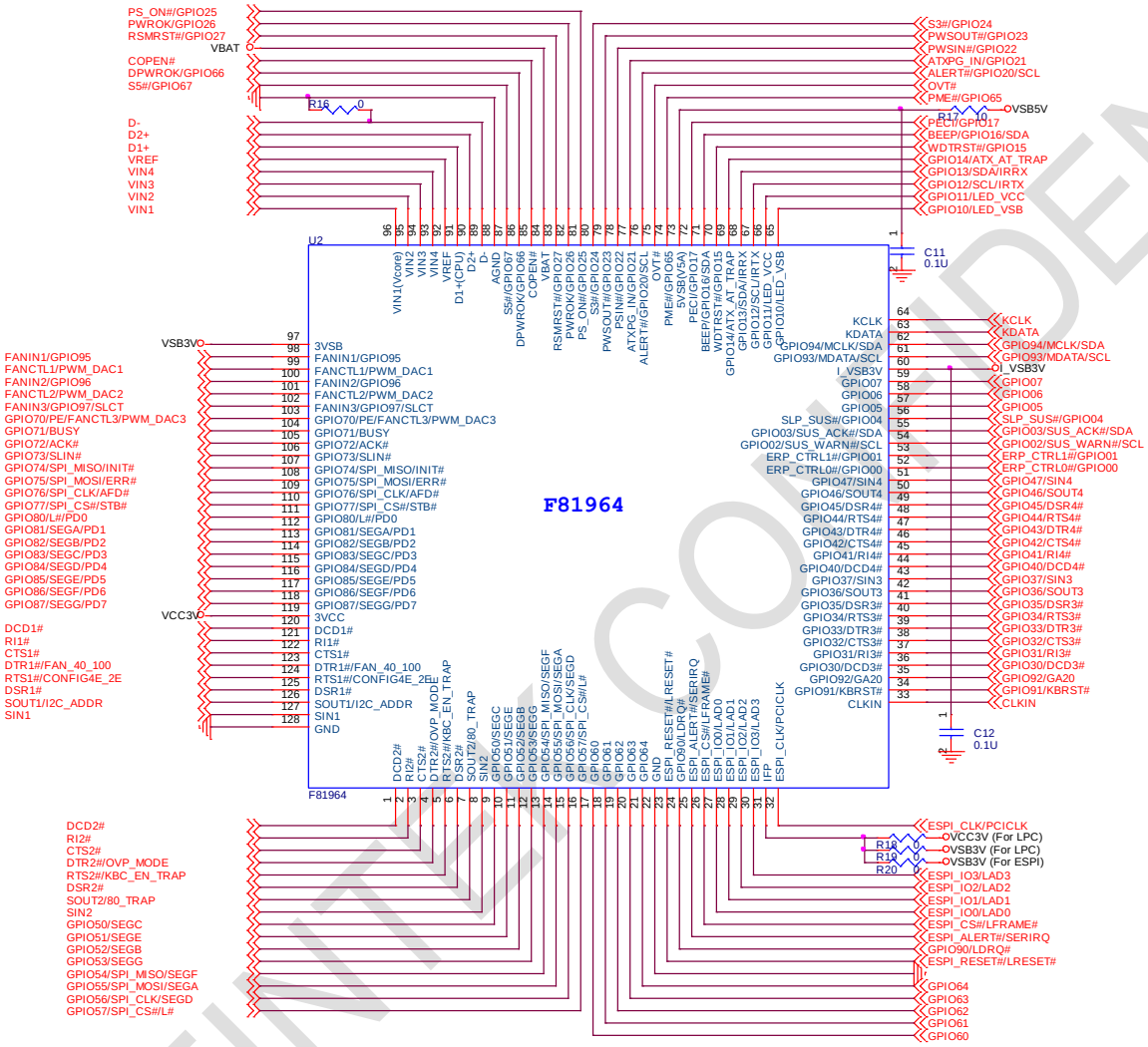
Date: Tuesday, February 06, 2018	Sheet 1 of 11	



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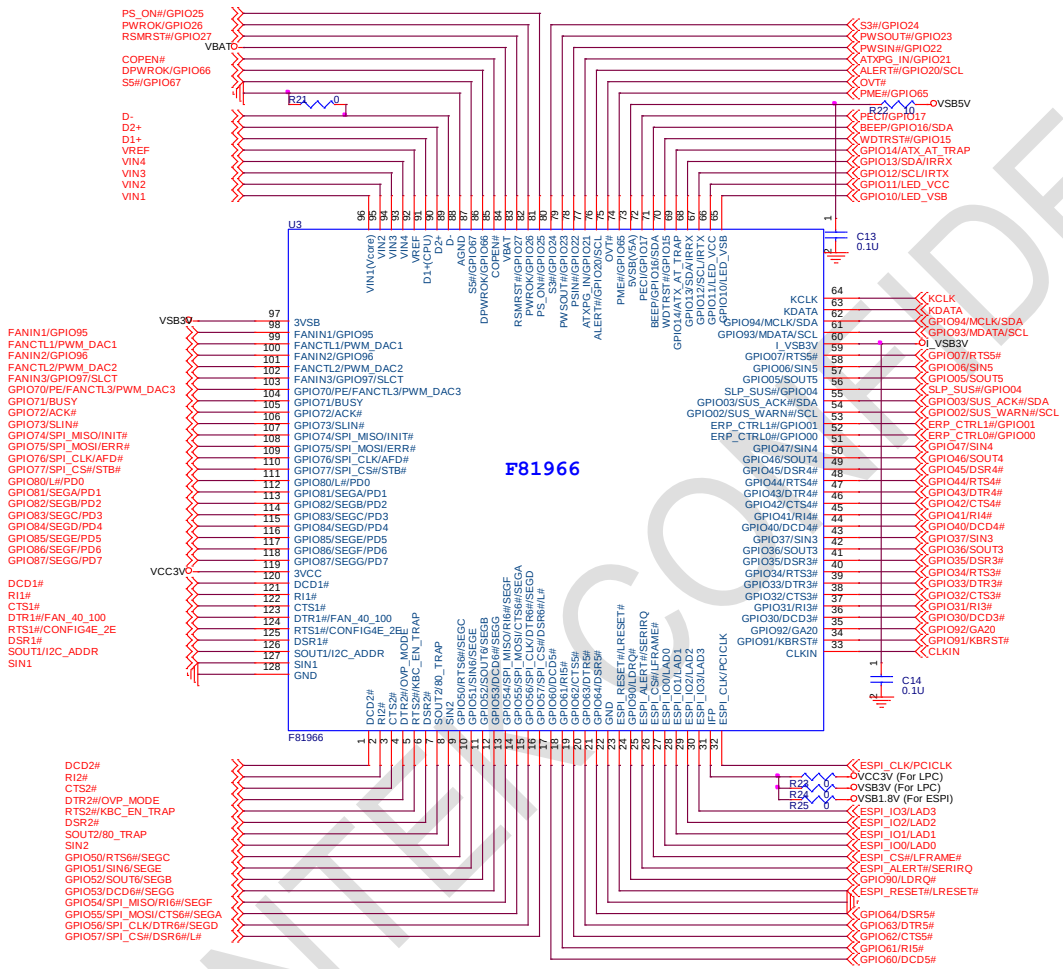
Size B	Document Number FINTEK		Rev <Rev Code>
Date: Tuesday, February 06, 2018	Sheet 2 of 11		



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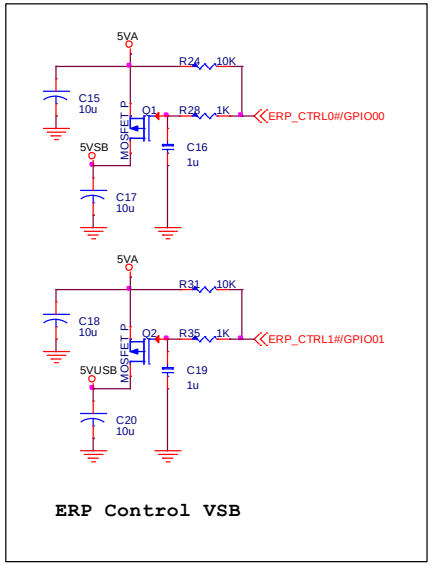
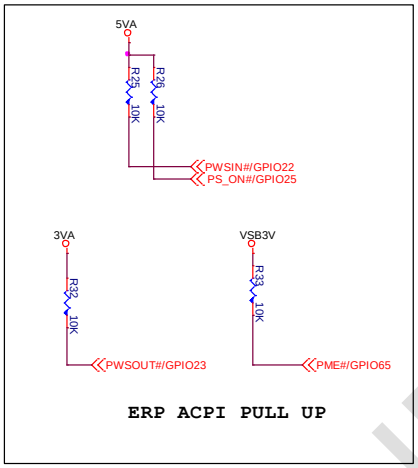
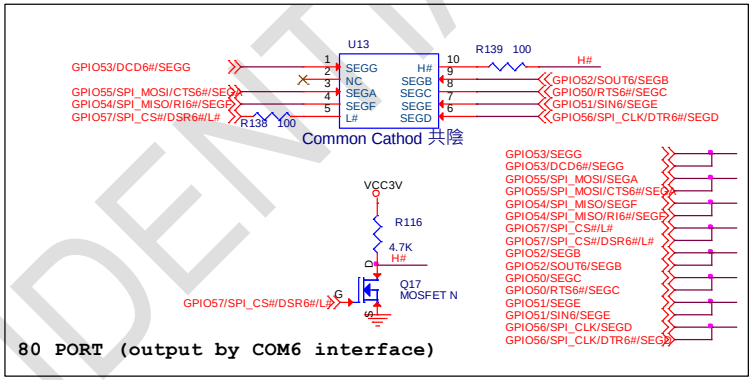
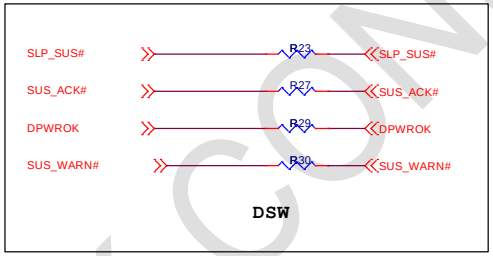
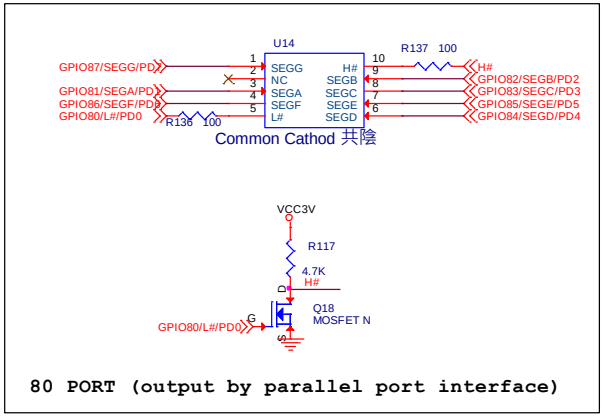
Date: Tuesday, February 06, 2018	Sheet 3 of 11	

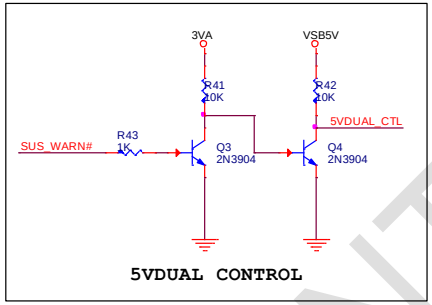


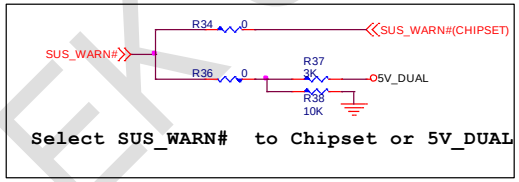


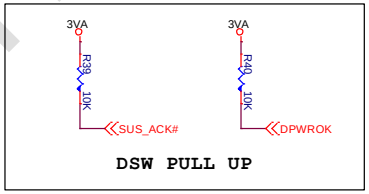












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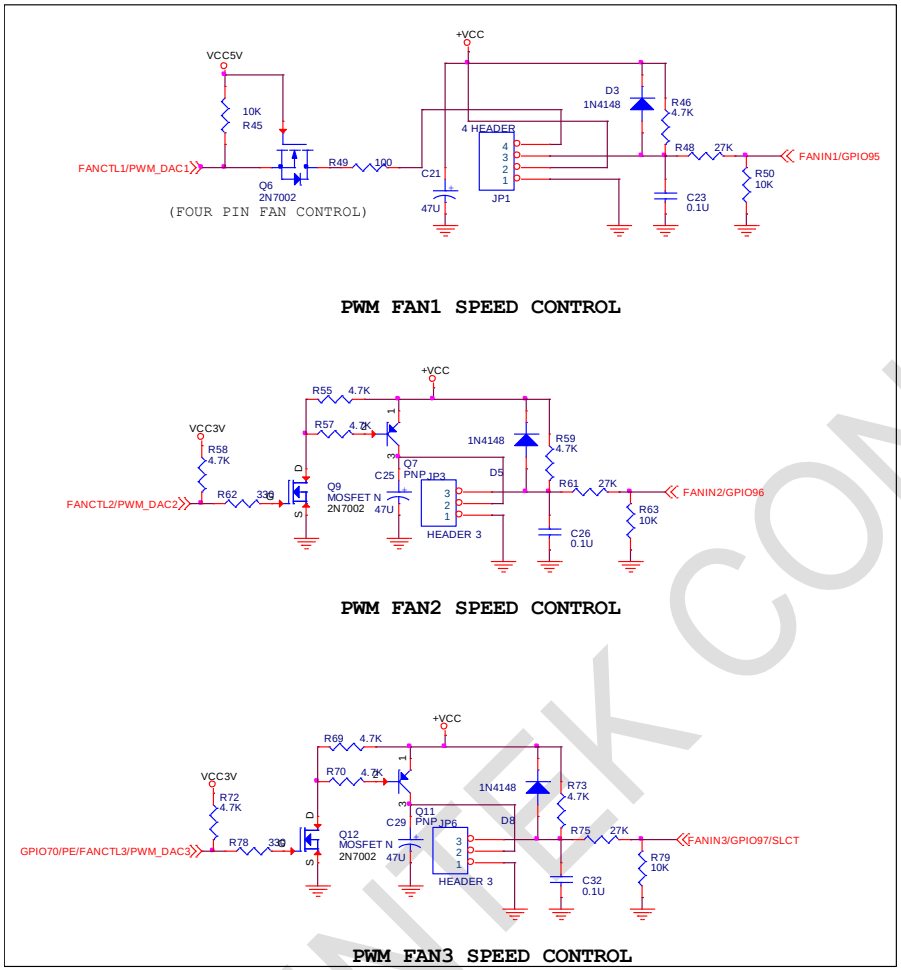

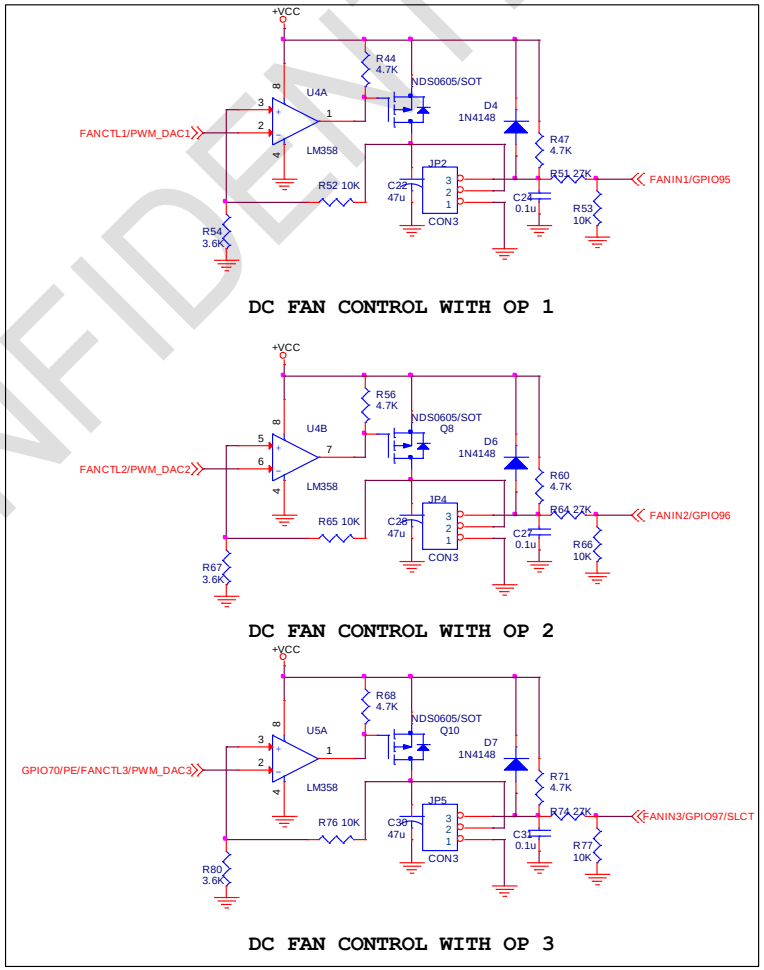

FAN CONTROL FOR PWM OR DC

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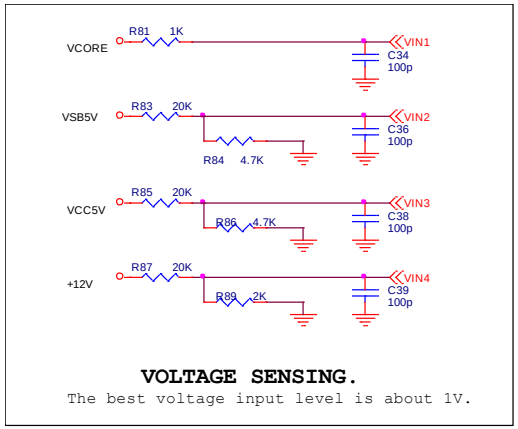
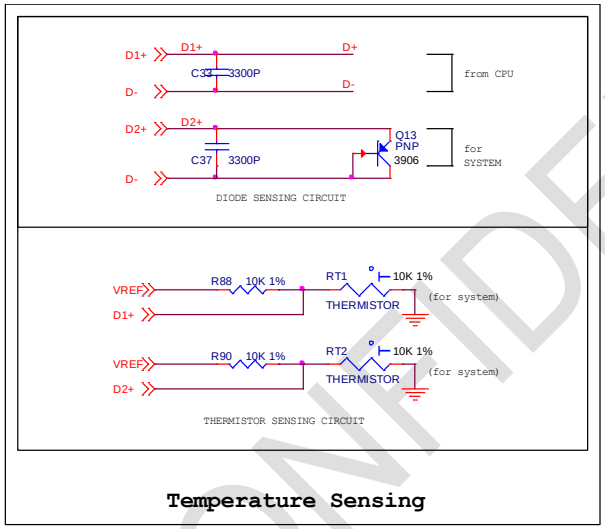
Date: Tuesday, March 21, 2017		Sheet 5 of 11	

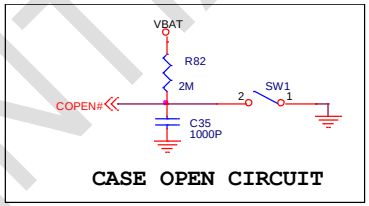


VOLTAGE SENSING.

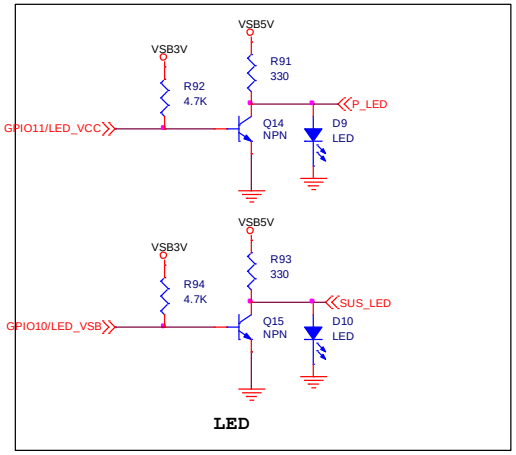
The best voltage input level is about 1V.



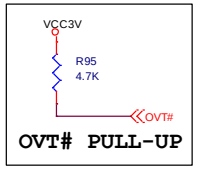
Temperature Sensing



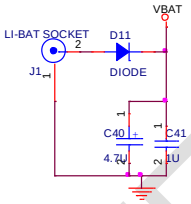
CASE OPEN CIRCUIT



LED



OVT# PULL-UP



Title	F81962/964/966 DEMO CIRCUIT	
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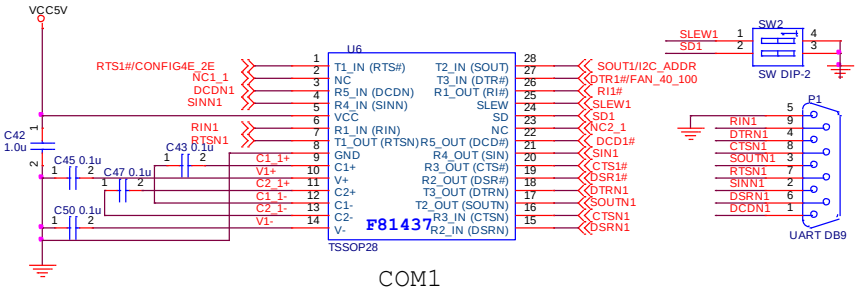

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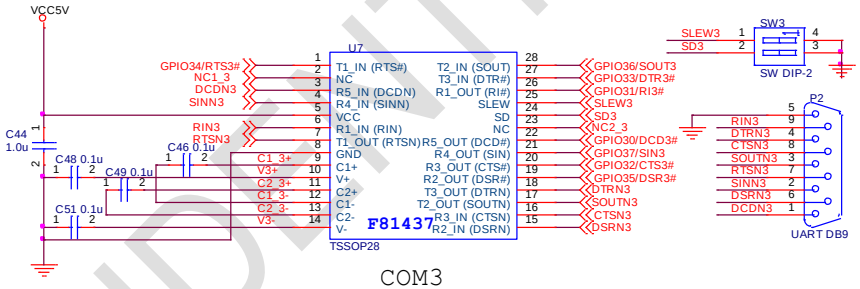

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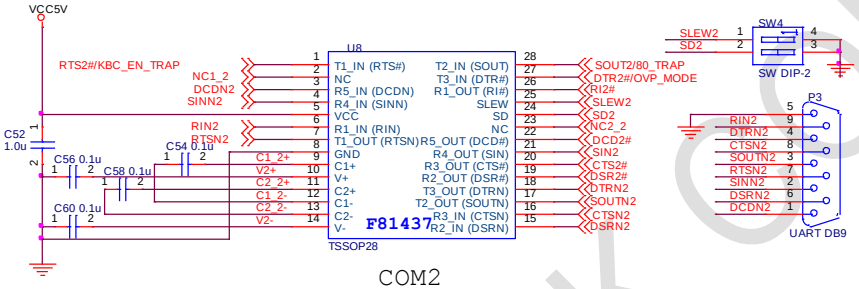

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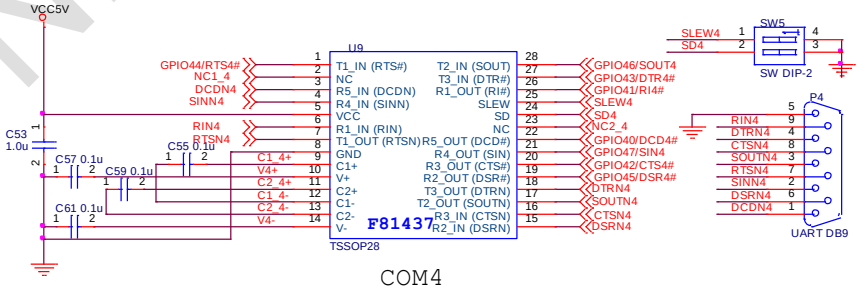

COM4

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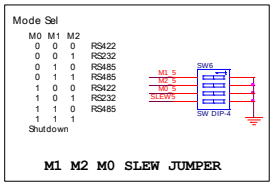
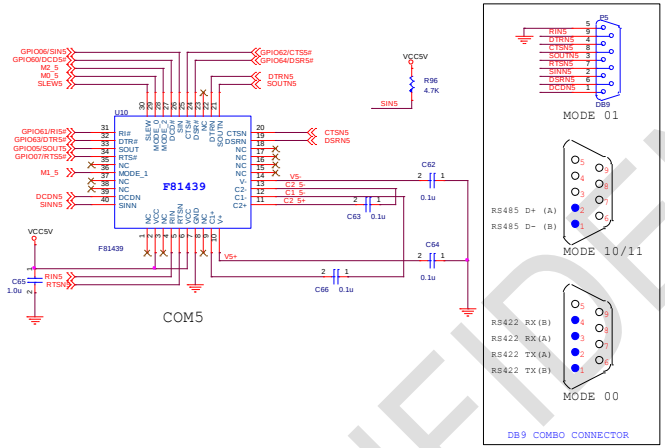
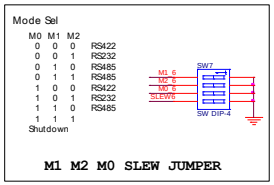
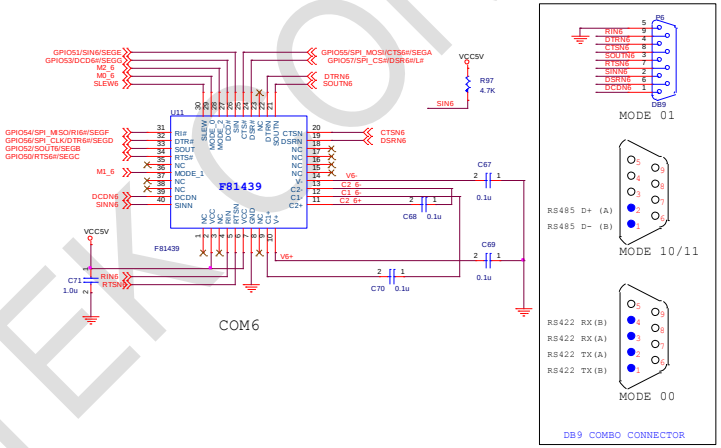
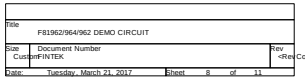
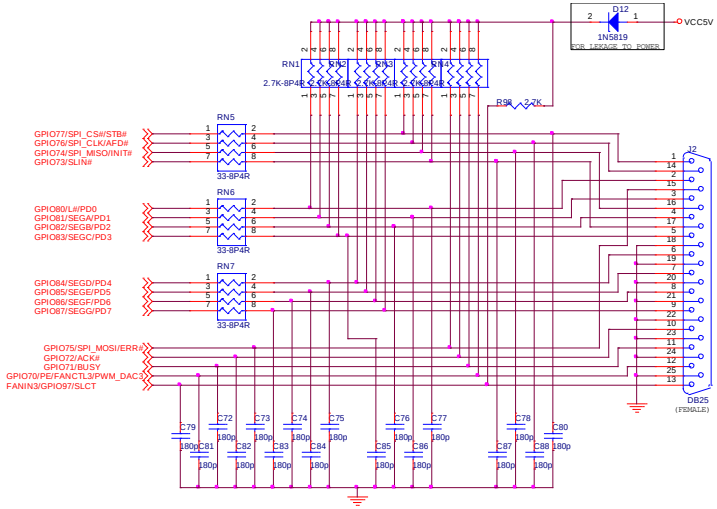




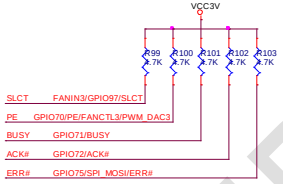




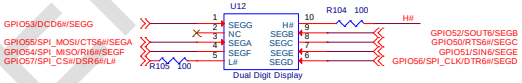


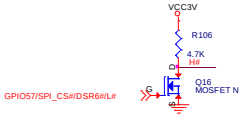


PARALLEL PORT INTERFACE

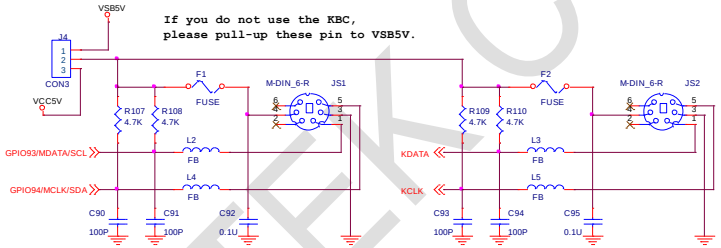


If you do not use the prarllel port , please pull-up these pin to VCC3V.





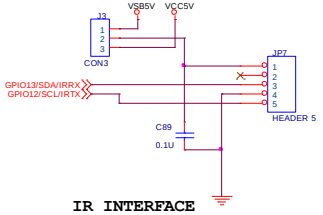
80 PORT



If you do not use the KBC, please pull-up these pin to VSB5V.

PS2 MOUSE INTERFACE

PS2 KEYBOARD INTERFACE



IR INTERFACE

Title	F81962/964/966 DEMO CIRCUIT		
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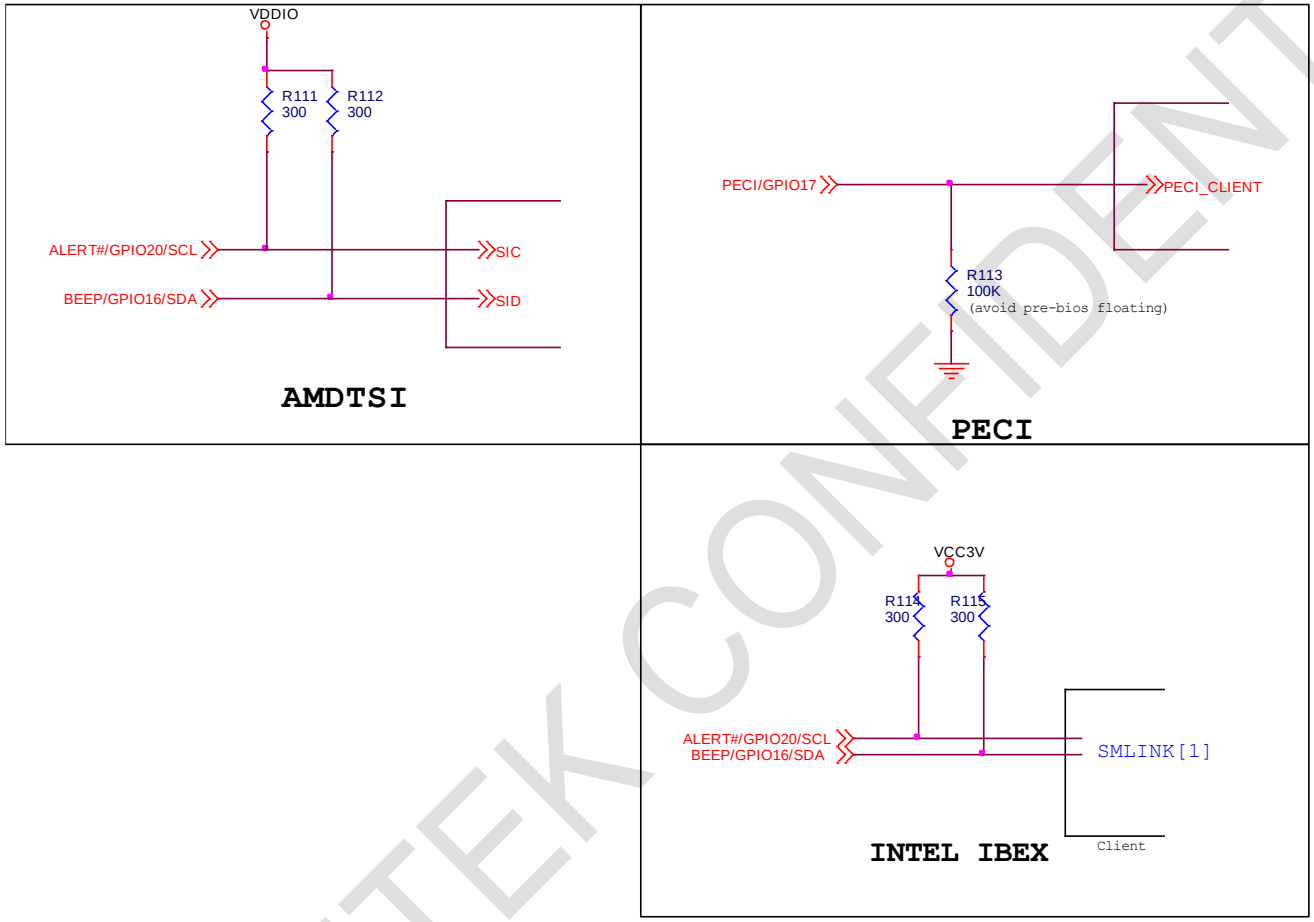

Title	F81962/964/966 DEMO CIRCUIT	
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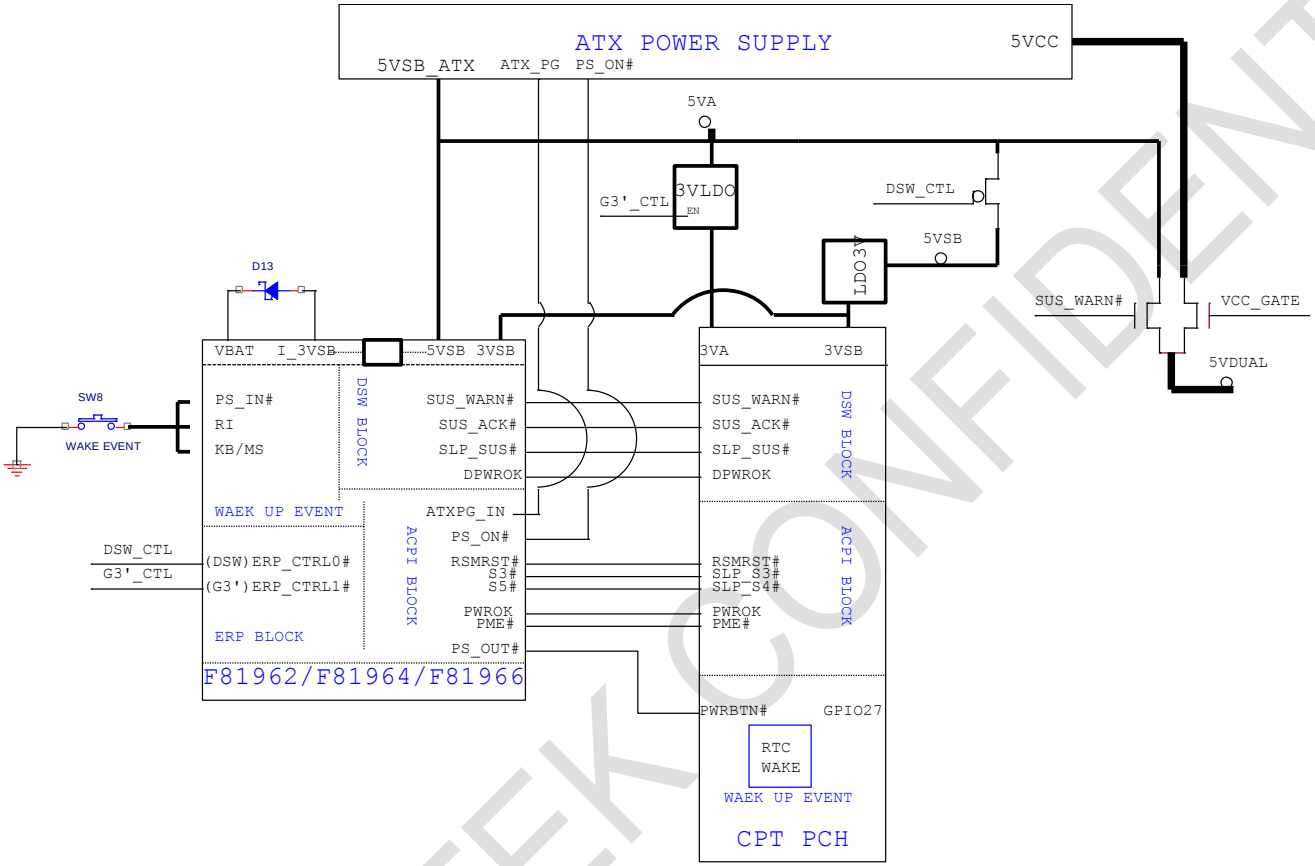

Title	F81962/964/966 DEMO CIRCUIT	
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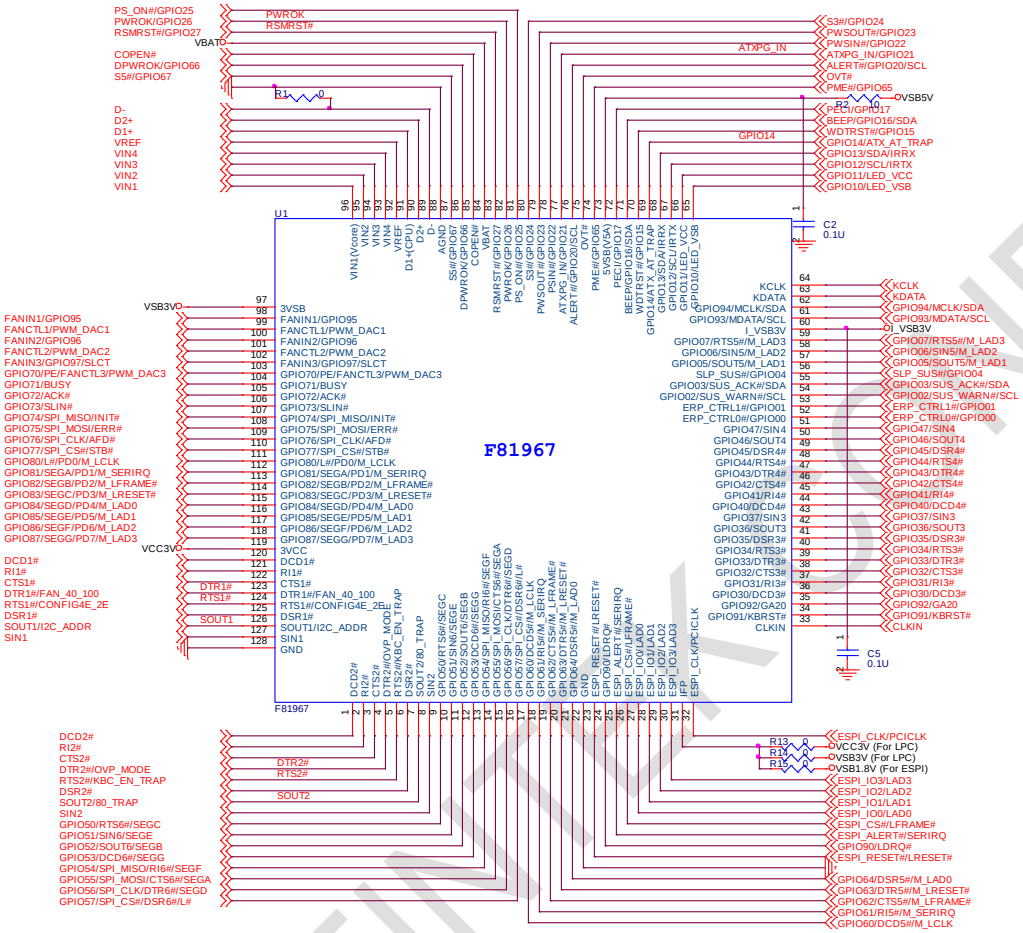
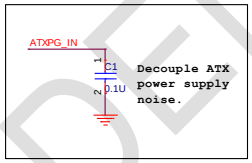
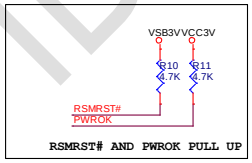
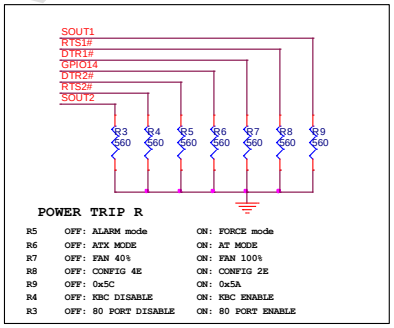
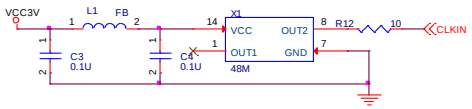
F81967 Application Circuit

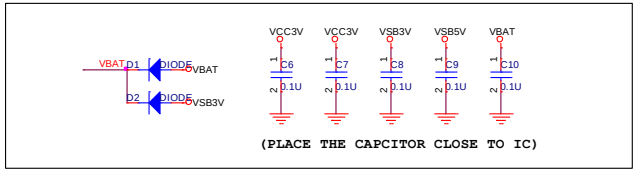












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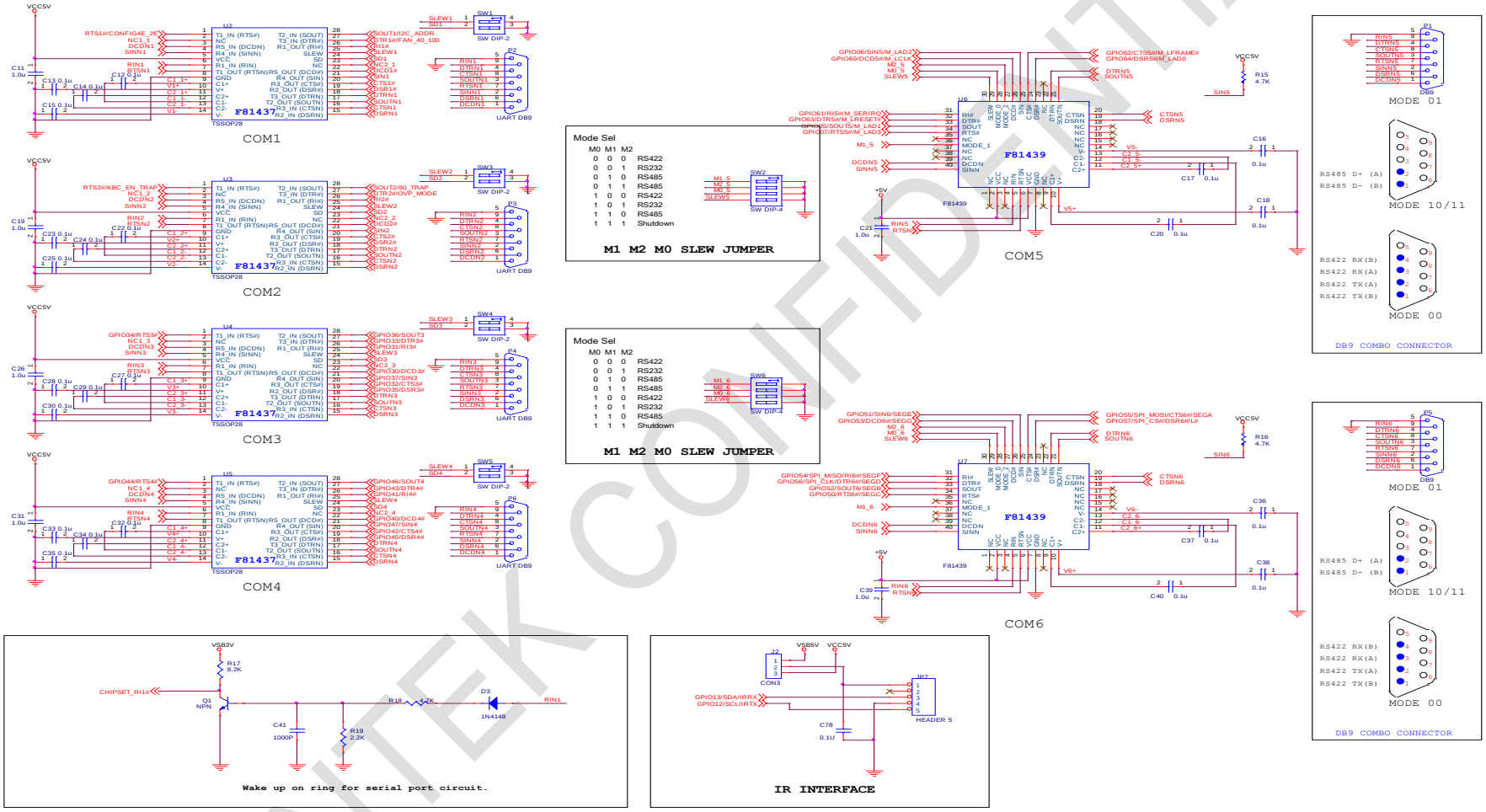

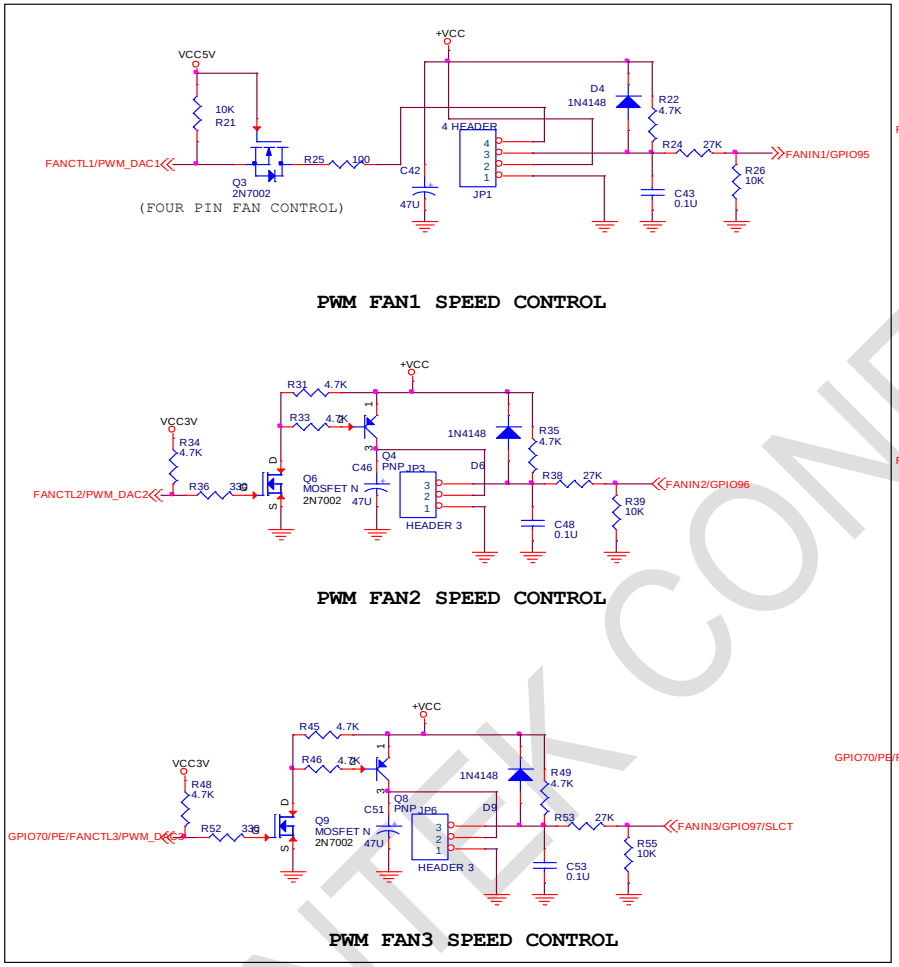

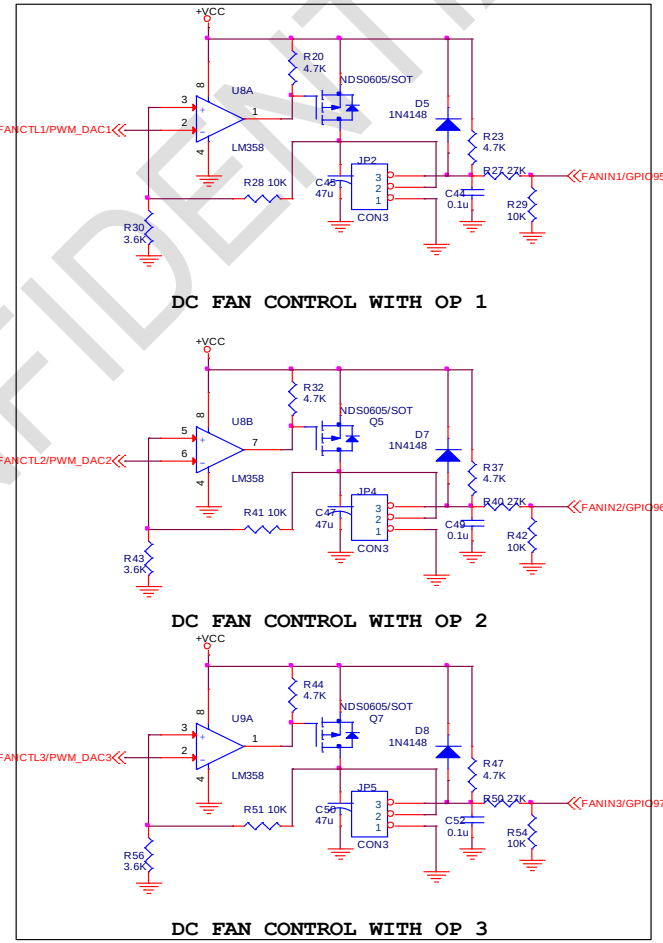

FAN CONTROL FOR PWM OR DC

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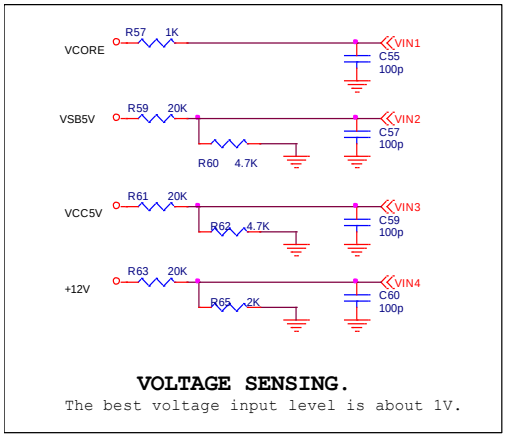
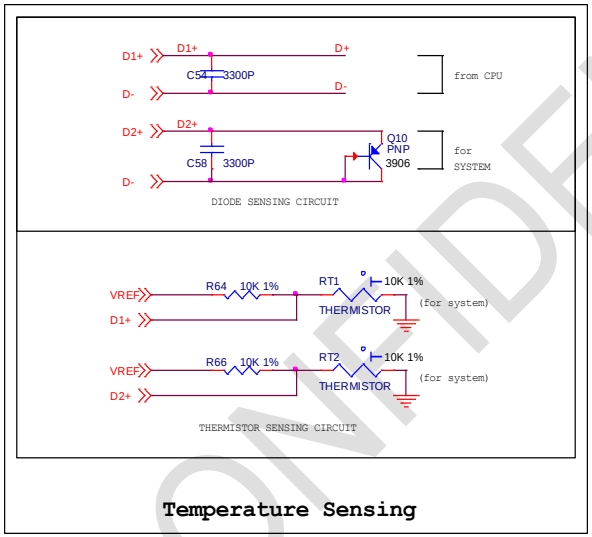
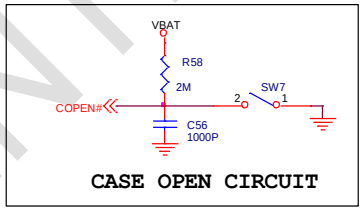


VOLTAGE SENSING.

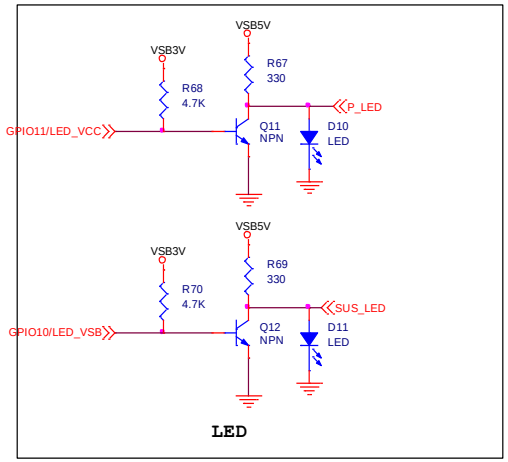
The best voltage input level is about 1V.



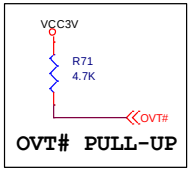
Temperature Sensing



CASE OPEN CIRCUIT



LED



OVT# PULL-UP

Title	Feature Integration Technology Inc.	
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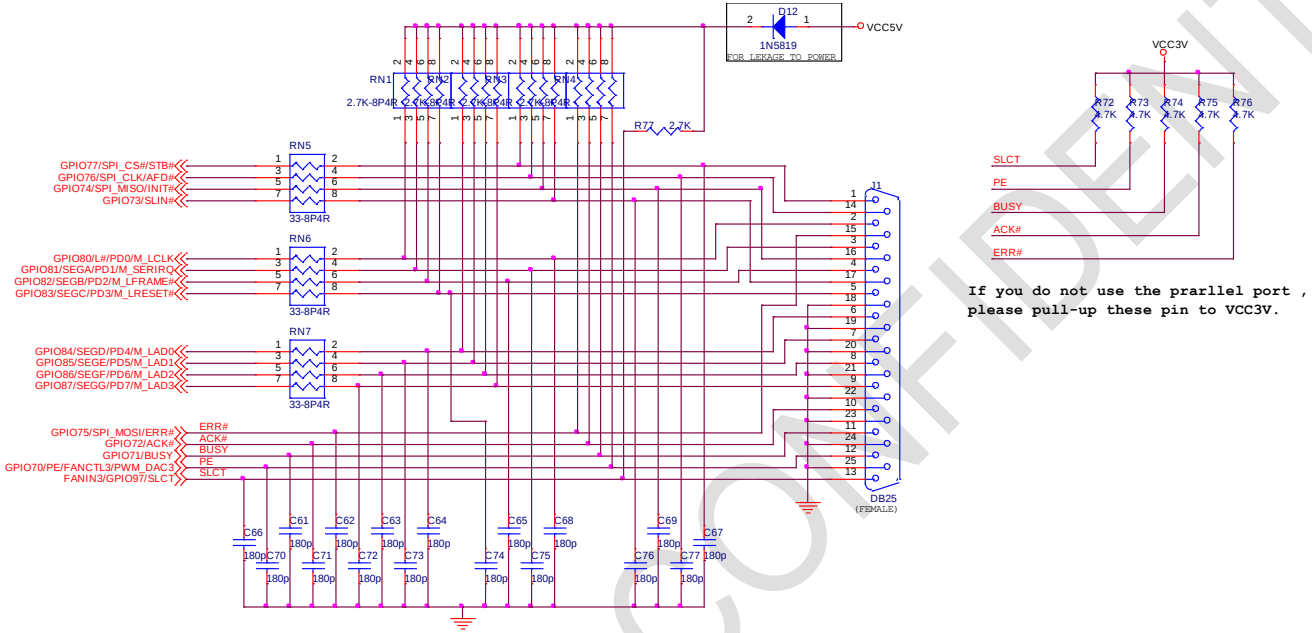
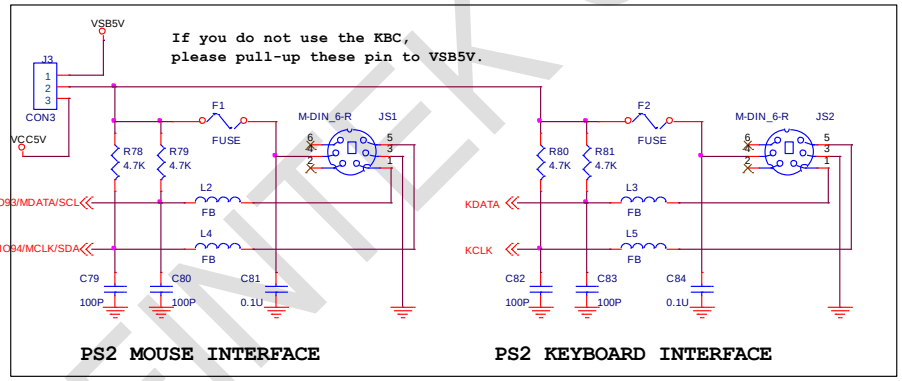


If you do not use the prarllel port , please pull-up these pin to VCC3V.

PARALLEL PORT INTERFACE



PS2 MOUSE INTERFACE **PS2 KEYBOARD INTERFACE**

Title	Feature Integration Technology Inc.		
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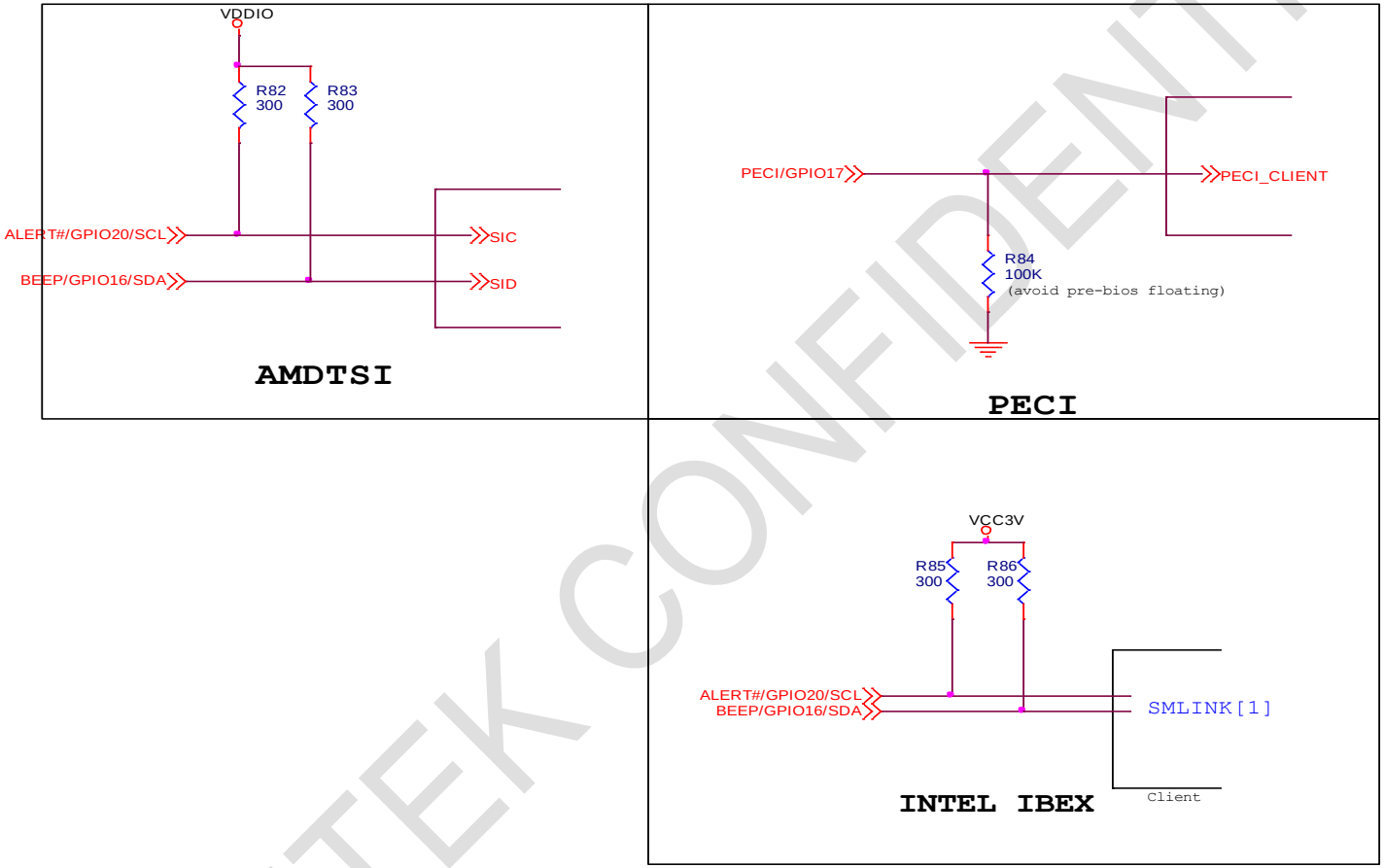

Title: Feature Integration Technology Inc.			
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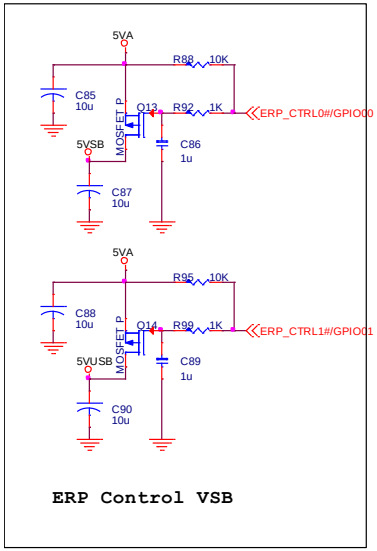

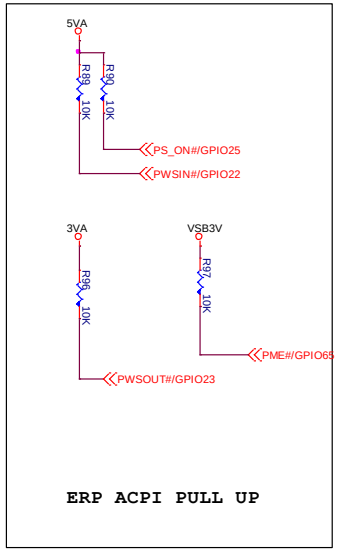

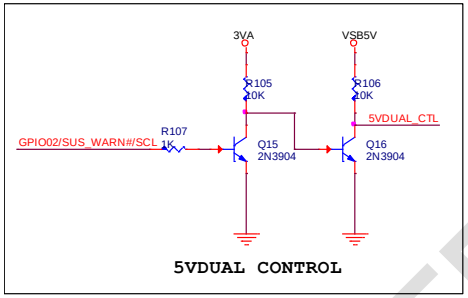

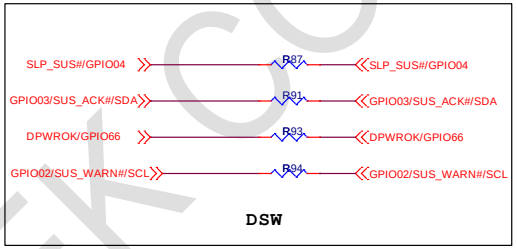

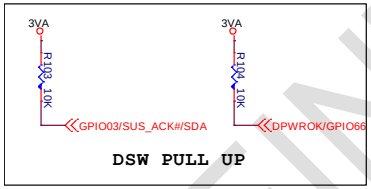

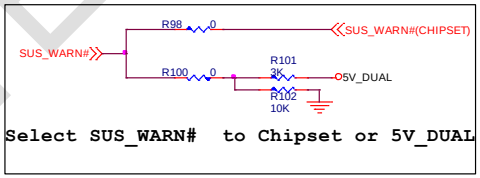

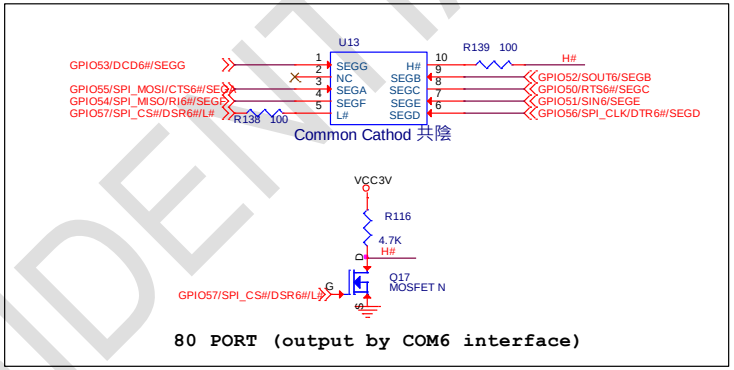

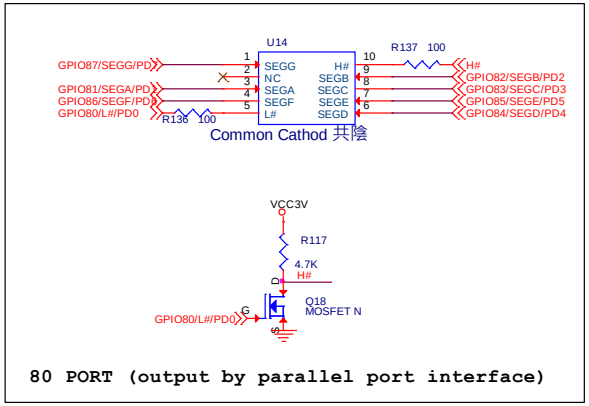

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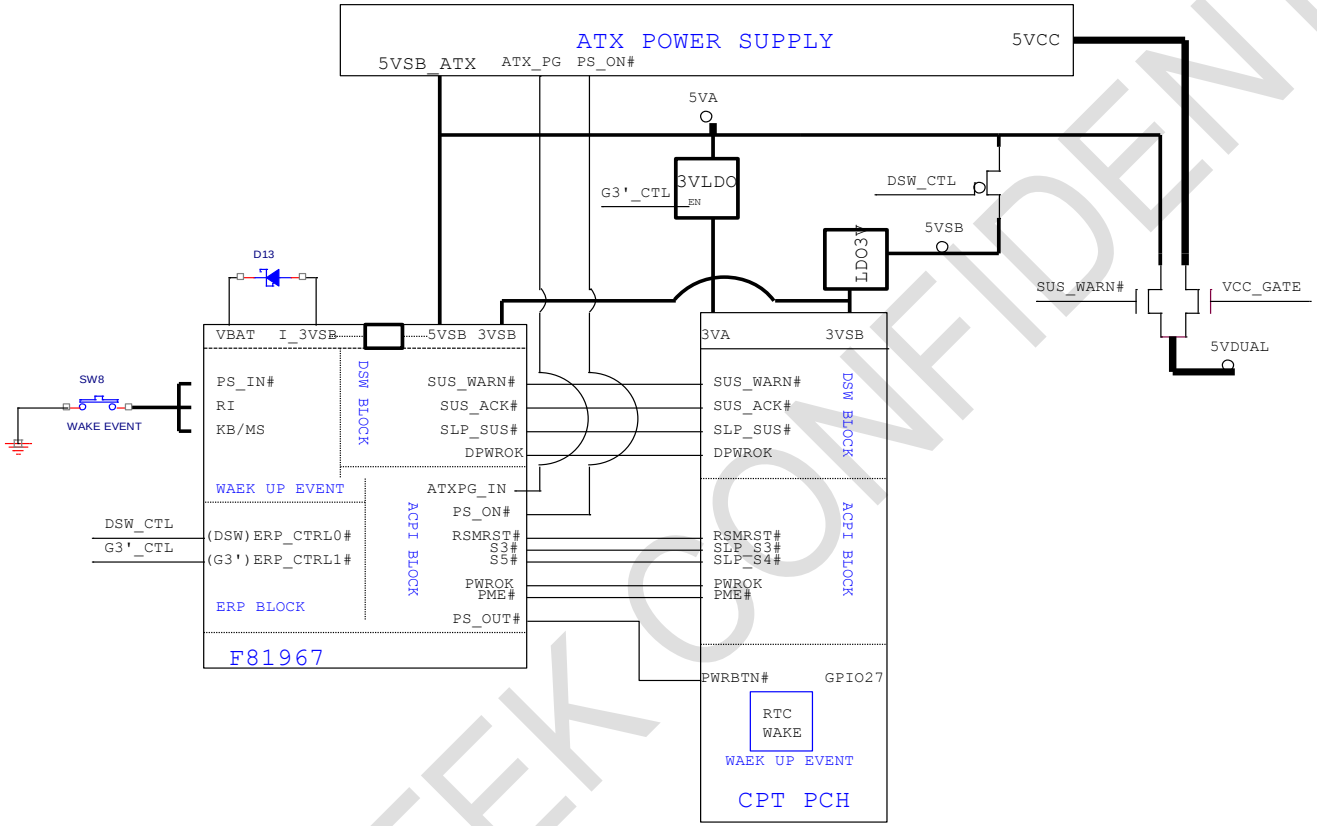

Title	Feature Integration Technology Inc.	
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